MMI/NATIONAL 303A-002 P/T ADAPTER

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NOTE

Before using this adapter, read the LogicPak™ Manual.*

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Applies to: Engineering Part Number 715-1965-007

Text Reference Number 090-0052

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SECTION 1
INTRODUCTION

1.1 OVERVIEW

The 303A-002 Monolithic Memories, Inc. (MMI)/National Semiconductor Corporation (National) programming/testing (P/T) adapter consists of one zero-insertion force socket with interface circuitry and EPROM (erasable, programmable read-only memory) mounted in a metal frame; see figure 1-1. The P/T adapter is used with the Data I/O 303A LogicPak™ to match programming electronics to the specific device family you are using. Any firmware unique to the MMI/National programmable logic devices is resident in the EPROM on the P/T adapter; all other necessary firmware is in the LogicPak™ or the programmer.

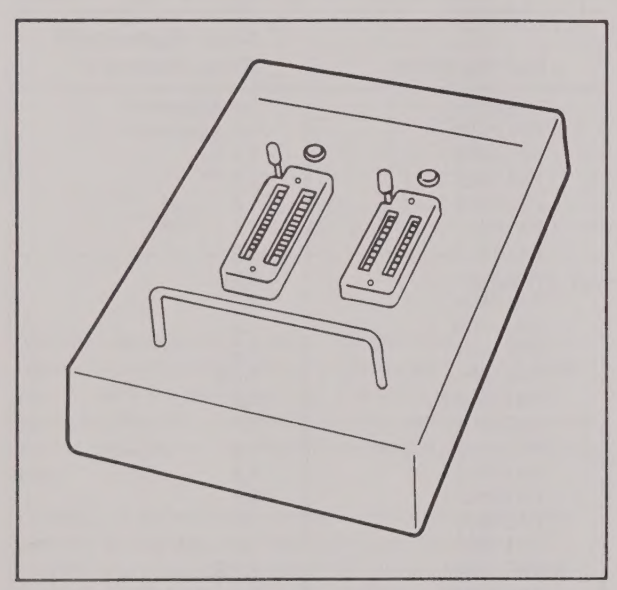

Figure 1-1. 303A-002 MMI/National Programming/ Testing Adapter

This manual describes how to use the MMI/National P/T adapter. Subjects addressed in this manual and their corresponding subsections are listed in table 1-1. Use this table as a quick-reference point for the major sections.

Table 1-1. Using the MMI/National Programming/ Testing Adapter Manual

SUBJECT	SECTION
Applications	1.2
Installation procedures for P/T adapter	2.2
Basic operation instructions	3.0
System commands	3.5
Calibration	4.2
Measurement chart for DC calibration tests	4.2
Error codes	4.2
Timing diagrams	4.2
Circuit description	5.0
Family and pinout codes	Appendix A
Logic diagrams	Appendix A
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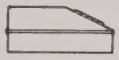
Warranty information	Back of manual

In this manual, we will refer to the operational procedures for the Model 29 Universal Programmer; refer to your programmer manual for System 19 and 100A key sequences.

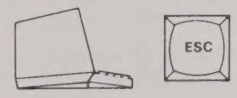
The entries that you are to make from either the programmer or the terminal are indicated by the symbols shown below:

TERMINAL MODE



PROGRAMMER FRONT PANEL

The following sequence indicates that the escape (*ESC*) key on the terminal keyboard should be pressed.



1.2 APPLICATIONS

Software tables resident within the P/T adapter store values for programming variables, including pinouts, voltage levels, and timing. When you choose the family and pinout codes for a particular device, the programmer uses information in these tables to assemble a specialized programming routine in scratch RAM (random-access memory). This allows high-speed operation with minimum firmware. Families with more than one pin number series (e.g., PAL®20 and PAL®24) have sockets to accommodate each pin count.

The family code and pinout code table (table A-1, appendix A) lists all the devices that can be programmed and/or tested with this P/T adapter. Table A-1 also lists the development aids as well as the family and pinout code corresponding to each device. This table will be updated as new devices are added. As Data I/O increases the capabilities of the LogicPak™ to program new devices, firmware and/or hardware updates will be available for existing adapters to add new devices to existing device families. New adapters will also be added to accommodate new-device families. Contact Data I/O for the latest revision and any required firmware updates.

If a fuse pattern is generated on a host system, it must use fuse numbers specified according to the logic diagrams in this manual and transmitted to the programmer in the JEDEC (Joint Electron Device Engineering Council) format (see appendix A of the LogicPak™ manual). Data I/O uses the JEDEC Logic Device Translation Format (number JC-42, 1-81-62) for serial data input and output with the LogicPak™. The only exception to this is when you are using a Signetics H&L design adapter, in which case data transfer can also occur in the Signetics H&L logic format.

NOTE

Before operating, see the JEDEC format specifications limitations in the LogicPak™ manual, appendix A.

1.3 DEVICE-SPECIFIC INFORMATION (LOGIC FINGERPRINT™ TEST LIMITATIONS)

The pseudo-random nature of the input vectors generated during the Logic Fingerprint™ test can cause some devices in some programming circumstances to fail by giving nonrepetitive results. This does not necessarily indicate a faulty device, but may be an indication that the device is subject to Logic Fingerprint™ test limitations. The device may still function in the system for which it was designed. The error flag indicating the Logic Fingerprint™ test failed is alerting you that this programmed pattern may not function for all possible input states.

Table 1-2 lists the devices and their Logic Fingerprint™ test limitations. Limitation 1 occurs when devices are programmed so that nonregistered outputs are fed back to product inputs, which results in an oscillation. This condition is shown in the simplified example in figure 1-2.

NOTE

Due to hardware limitations, fingerprint cannot be used on the PAL8L14 and PAL6L16.

Table 1-2. Logic Fingerprint™ Test Limitations for MMI/National Programmable Logic Devices

Part Numbers	Logic Fingerprint™ Test Limitations
PAL6L16	not supported
PAL8L14	not supported
PAL10H8	1,2
PAL10L8	1,2
PAL12H6	1,2
PAL12L6	1,2
PAL12L10	1,2
PAL14H4	1,2
PAL14L4	1,2
PAL14H8	1,2
PAL14L8	1,2
PAL16A4	1,2,3
PAL16C1	1,2
PAL16H2	1,2
PAL16L2	1,2
PAL16L6	1,2
PAL16L8	1,2
PAL16L8B	1,2
PAL16P8	1,2
PAL16R4	1,2,3
PAL16R4B	1,2,3
PAL16R6	1,2,3
PAL16R6B	1,2,3
PAL16R8	1,2,3
PAL16R8B	1,2,3
PAL16RP4	1,2,3
PAL16RP6	1,2,3
PAL16RP8	1,2,3
PAL16X4	1,2,3
PAL18L4	1,2
PAL20C1	1,2
PAL20L2	1,2
PAL20L8	1,2
PAL20L10	1,2
PAL20R4	1,2,3
PAL20R6	1,2,3
PAL20R8	1,2,3
PAL20RA10	1,2,3
PAL20RS4	1,2,3
PAL20RS8	1,2,3
PAL20RS10	1,2,3
PAL20S10	1,2,3
PAL20X4	1,2,3
PAL20X8	1,2,3
PAL20X10	1,2,3

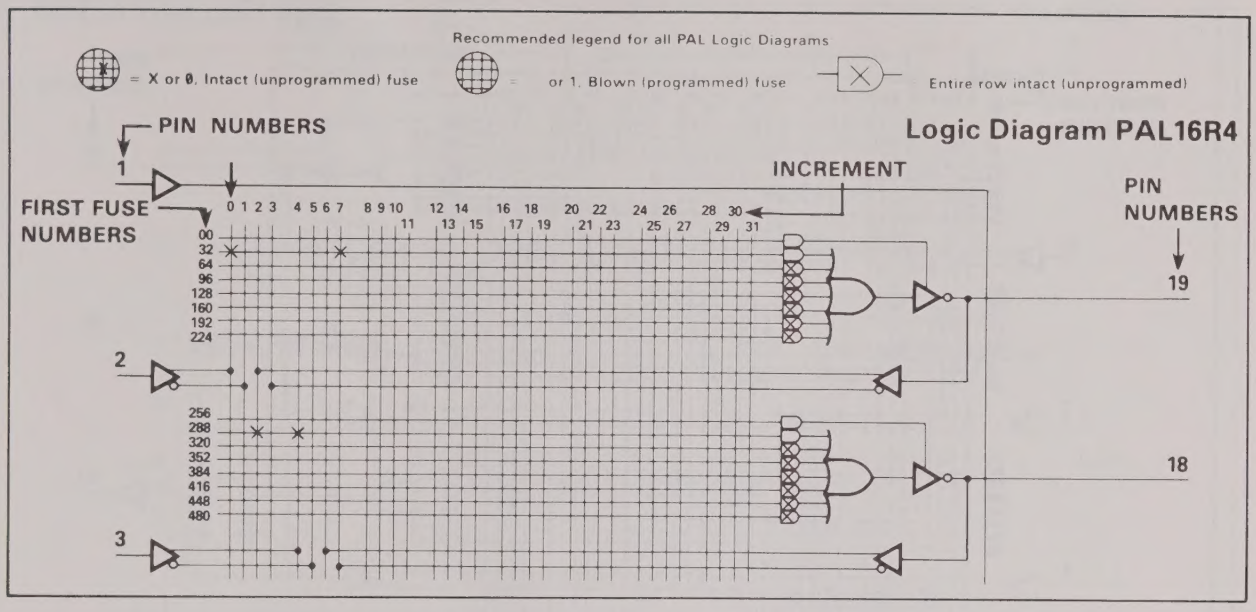


Figure 1-2. Example of Limitation 1

The two nonregistered product outputs (pins 18 and 19) in figure 1-2 feed back to the other product's input. If input pins 2 and 3 are both true (i.e., TTL "1"), the PAL will oscillate. This condition could exist for one product output feeding back to its own input or numerous outputs feeding back.

Limitation 2 occurs when a race condition is programmed into the device. Because the inputs are controlled, it is possible that the race condition will not be critical in the circuit for which the device was designed. Due to the random nature of the inputs during the Logic Fingerprint™ test, the race condition could appear and cause unstable results. An RS latch is an example of this. Figures 1-3 and 1-4 show the schematic, truth table, Boolean equations, and fuse map. Suppose that A, B, and C are at logic lows, 01 is at a logic high, and 02 is at a logic low. Let B and C go to a logic high simultaneously. The state of S will depend on how fast B and C can propagate through the logic gates. The effect of B will arrive at S first, forcing it low. At a time equal to the propagation delay of the gates later, the effect of C will be seen at S, forcing it back to a logic high. When S was at a logic low, the RS latch changed state and is unaffected when S comes back high. This causes the Logic Fingerprint™ test to read the wrong values on the outputs, which in turn causes an unstable result.

If the default starting vector of Ø results in a test-sum of *FFFFFFFF*, select a starting vector other than Ø.

Limitation 3 occurs in registered parts only. When using the Logic Fingerprint™ test, you must start from the same state every time the test is performed. These registered PALs, however, will not power up into the same state every time the test is performed. If the Logic Fingerprint™ test starts at a different point, it will produce unstable results. To overcome this limitation, the registered outputs must be put into a known state before executing the Logic Fingerprint™ test. Two methods of doing this are:

1. Dedicate one input line as a preset or reset line for all registered output. A starting vector can then be written to set or clear all registered outputs.
2. If no extra inputs are available to dedicate to a preset/reset line or a known state of other than all ones or all zeros is required, the setup must consist of one or more vectors to force the outputs into the desired state. If more than one is needed, the structured test must be used to input the vectors rather than the starting seed for the Logic Fingerprint™ test. (See LogicPak™ manual, subsection 1.4.3 and this manual, subsections 3.5.7 and 3.5.8.)

The VØ3 and later versions of the 303A-002 P/T adapter have added a feature which greatly improves Logic Fingerprint™ testing of MMI registered PALs®. It contains a routine which automatically presets the registers in the PAL prior to the Logic Fingerprint™ test. (See subsection 3.6 for more information.)

NOTE

It is important that you recognize when devices are programmed with these limitations and realize that the Logic Fingerprint™ test will reject them. These devices can still be tested by using structured test vectors.

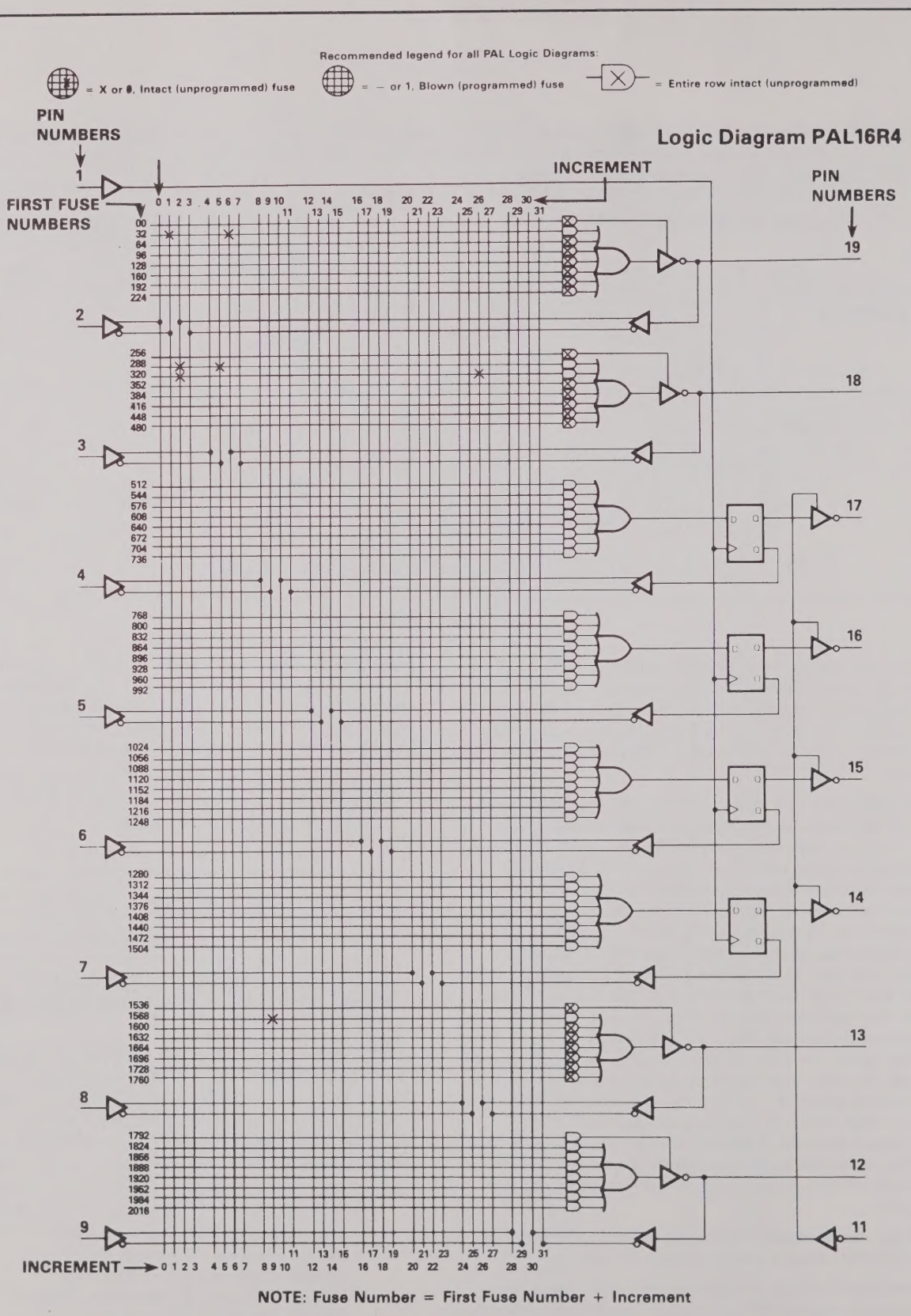
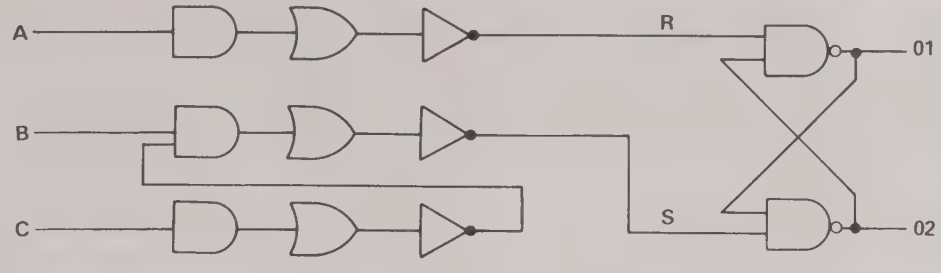


Figure 1-3. Example of Limitation 2



RS TRUTH TABLE

R	S	01	02
0	0	1	1
0	1	1	0
1	0	0	1
1	1	a	a

[a] Remains unchanged

BOOLEAN EQUATIONS

$01 = \overline{02 * R}$

$02 = \overline{01 * S}$

$\boxed{\overline{01} = 02 * \bar{A}}$

$\overline{02} = 01 * [\overline{B * \bar{C}}]$

$01 * [\bar{B} + C]$

$\boxed{\overline{02} = (01 * \bar{B}) + (01 * C)}$

$R = \bar{A}$

$S = \overline{B * \bar{C}}$

Figure 1-4. Example of Limitation 2 With Truth Table and Boolean Equations

1.4 SPECIFICATIONS

The P/T adapter receives its power from the LogicPak™ and the programmer power supplies. Programming waveforms are generated from programmer supplies using the digital-to-analog converters (DAC) controlled by the programmer's microprocessor. The controlling firmware is located both on a circuit board in the LogicPak™ and in the P/T adapters. The physical and environmental specifications of the P/T adapter are:

- Altitude (operating): sea level to 3 km (10,000 ft)
- Humidity (operating): 90% maximum (noncondensing)
- Humidity (storage): 95% maximum (noncondensing)
- Temperature (operating): +5 to 45°C (41 to 113°F)
- Temperature (storage): −40 to 70°C (−40 to 158°F)
- Weight: 0.255 kg (9 oz)
- Dimensions: 16.6 x 12.3 x 2.1 cm (6.54 x 4.84 x 0.81 in.)

1.5 FIELD APPLICATIONS SUPPORT

Data I/O has field applications engineers throughout the world. They can provide additional information about interfacing Data I/O products with other systems and answer questions about your equipment.

The engineers within the United States are located at the addresses listed in the back of this manual. For international applications support, contact your nearest Data I/O representative.

1.6 WARRANTY

The 303A-002 P/T adapter is warranted against defects in materials and workmanship. The warranty period of one year begins when you receive the equipment; the warranty card inside the back cover of this manual explains the length and conditions of the warranty. For warranty service, contact your nearest Data I/O service center.

1.7 SERVICE

Data I/O maintains service centers throughout the world, each staffed with factory-trained technicians to provide prompt, quality service. A list of all service centers is located in the back of this manual.

1.8 ORDERING

To place an order for equipment, contact your Data I/O sales representative. Orders for shipment must include:

- A description of the equipment. (See the latest Data I/O price list or contact your sales representative for equipment and part numbers.)
- Purchase order number.
- Desired method of shipment.
- Quantity of each item ordered.
- Shipping and billing address of the firm, including ZIP code.
- Name of person ordering the equipment.

SECTION 2
INSTALLATION

2.1 INSPECTION

The P/T adapter was thoroughly tested and inspected before shipment and was carefully packaged to prevent shipping damage. Inspect your adapter to ensure that no damage occurred during shipment. If you notice any damage, file a claim with the carrier and notify Data I/O.

2.2 ADAPTER INSTALLATION

To insert the P/T adapter into the LogicPak™:

1. Check to make sure a device is not in the socket. If a device is in the socket, remove it as described in subsection 3.4.3.
2. Align the guide pins on the underside of the adapter with the guide pin holes on the LogicPak™ (see figure 2-1).
3. Gently set the adapter on the LogicPak™.
4. Firmly press down on the front edge of the adapter to lock the connector pins into the connector receptacle (see figure 2-1).

2.3 ADAPTER REMOVAL

CAUTION

Before removing the adapter, you must return control to the programmer. This is done by pressing *ESC* at the terminal, *KEYBOARD* on the System 19, or *VERIFY* on the 100A or Model 29. Because the processor in the programmer executes firmware resident in the adapter, these precautions must be taken before removing the adapter from the LogicPak™ to prevent program interruption and possible loss of RAM data.

To remove the adapter:

1. Ensure that the programmer has completed the current operation.

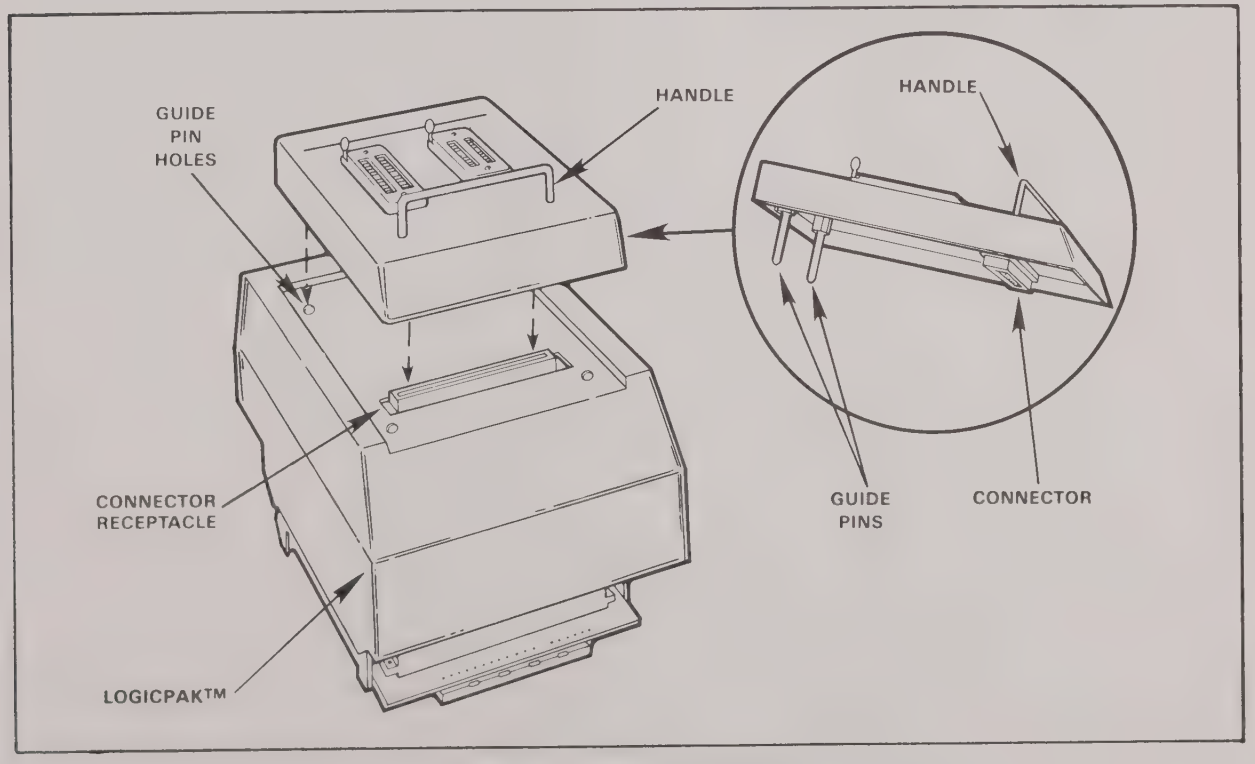


Figure 2-1. Adapter Installation

2. Ensure that a device is not in a socket.
3. While holding down the LogicPak™, grasp the adapter handle and gently remove the adapter.

2.4 REPACKING FOR SHIPMENT

If the adapter is to be shipped to Data I/O for service or repair, attach a tag to it describing the work required and identifying the owner. In correspondence, identify the unit by part number, revision level, and the name of the unit. If the original shipping container is to be used, place the adapter in the container with the appropriate packing materials, and seal the container with strong tape. If another container is used, be sure that it is a heavy carton, wrapped with heavy paper or plastic; use appropriate packing material, and seal well with strong tape. Mark the container "DELICATE INSTRUMENT" or "FRAGILE."

SECTION 3
OPERATION

3.1 OVERVIEW

The 303A-002 P/T adapter enables you to program and functionally test the MMI/National devices listed in table A-1 of appendix A. These logic devices are arrays of gates and flip-flops joined by matrices of fusible links. The devices can be programmed by blowing selected fuses in the matrices, which leaves the remaining intact connections to perform the desired logic functions.

The fuse pattern necessary to program a device should already have been developed using a Data I/O LogicPak™ and a design adapter or a host computer system; if you have not developed your fuse pattern, consult the LogicPak™ manual and design adapter manual to develop your data before proceeding. However, if you have entered your data in Boolean equations or function tables (truth tables), they must be translated into a fuse pattern before you can begin programming. (Don't turn the power off; if you do, you will lose all your data.) If you have not used a design adapter, the fuse pattern must be loaded from: 1) a master device, 2) the serial port, or 3) manually from a programmer or terminal keyboard.

An alternate method of specifying the fuse pattern is to manually enter the fuse number and state for every fuse in the device. Appendix A contains logic diagrams for the MMI/National devices in its repertoire. These are the same as those in the device manufacturer's data book, but the fuse numbers have been added. Although the method is tedious, fuse numbers and states can be entered manually into the programmer's data RAM from the programmer's keyboard or from a terminal. This method usually will be used only for editing fuse data because it is a long process with room for error.

With a P/T adapter, fuse data can be entered into the programmer's RAM by loading from a master device. Blank devices can then be programmed using the same P/T adapter, or other manufacturers' functionally equivalent second-source devices can be programmed by installing the appropriate P/T adapter.

Programming is controlled either from the programmer keyboard or from a terminal. Firmware in the P/T adapter automatically tests the device's position in the socket, ensures that the device is blank, and looks for illegal bits; figure 3-1 defines the overall fuse programming sequence. Programming begins when these automatic checks are completed and determined acceptable.

After the device has been programmed, it is automatically verified and tested according to options you select. See subsection 3.5.5.

In addition to enabling you to program and test devices, the P/T adapter also enables you to view data, change them, and/or enter test parameters. These optional steps are listed in table 3-1. The functions of the P/T adapter are described in table 3-1 and subsection 3.5. Sections 1 and 3 of the LogicPak™ manual also describe these functions. Logic diagrams with decimal fuse numbers are in appendix A of this manual.

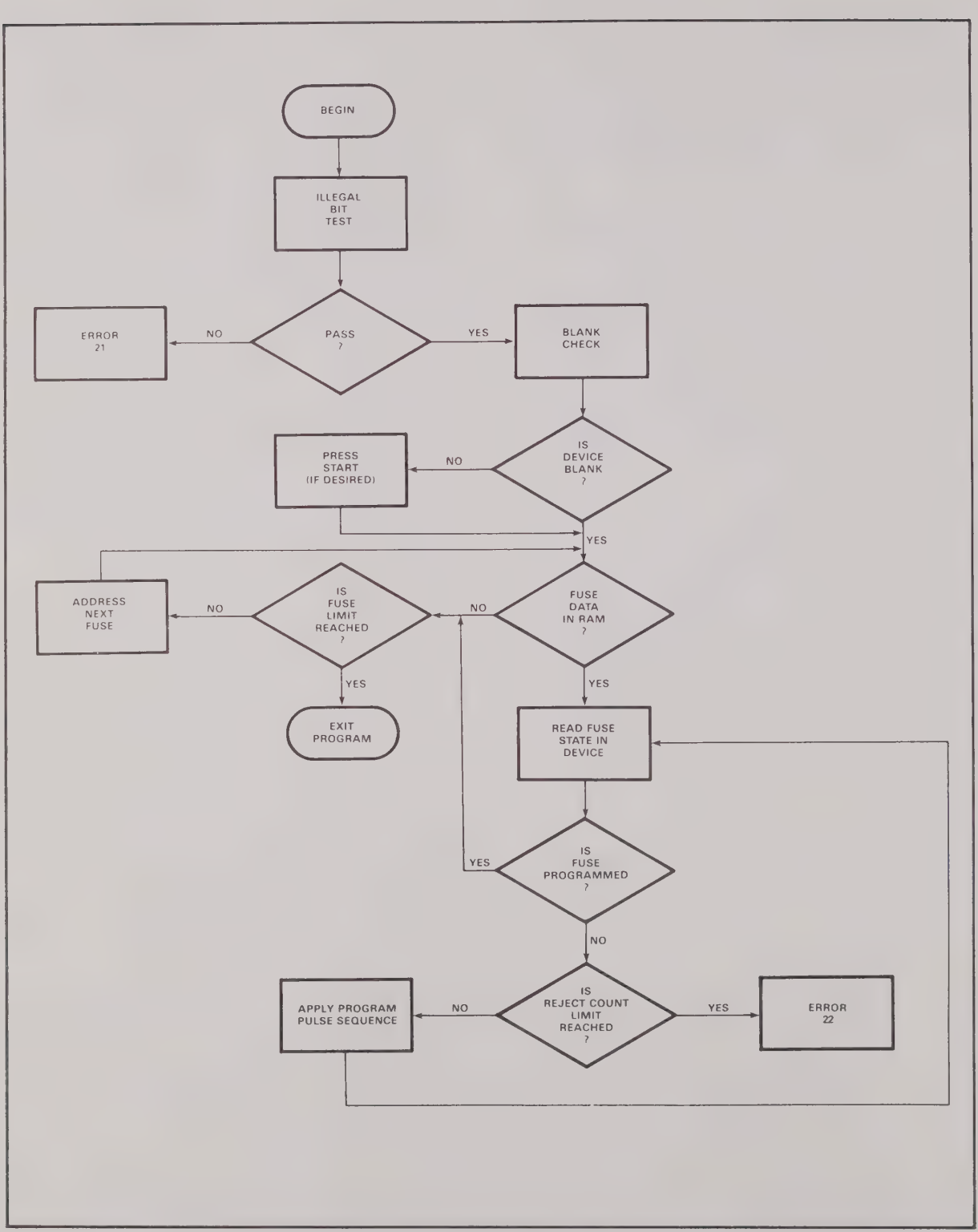


Figure 3-1. Automatic Programming Sequence Flow Chart

Table 3-1. PLDS Command Summary

MODULE OR ADAPTER	COMMAND TYPE	FROM FRONT PANEL	VIA TERMINAL	COMMAND DESCRIPTION	SEE SUBSECTION
LogicPak™ (with any adapter)		--	Ø	Display menu	3.5.2
		E 1	--	Enable terminal mode	3.5.1
		--	1	Enter family code and pinout code	3.5.3
		E 5[a]	5[a]	Enter reject count option	3.5.4
		E 6	6	Enter verify option	3.5.5
		E 7	7	Enter security fuse option	3.5.6
		E 8	8	Set number of Logic Fingerprint™ test cycles	3.5.7
		E 9	8	Enter starting vector and test-sum	3.5.7
		--	8	Enter structured test vectors	3.5.7
				Ø Display menu	3.5.7
				D Delete current vector	3.5.7
				R Repeat current vector	3.5.7
				U Display previous vector	3.5.7
				#(N) Go to vector (N)	3.5.7
				space Move cursor right	3.5.7
				backspace[b] Move cursor left	3.5.7
				return Display next vector	3.5.7
				CTRL Z Exit vector editor	3.5.7
		E A	A	Display fuse pattern	3.5.8
		E B	B	Receive JEDEC data	3.5.9
		E C	C	Transmit JEDEC data	3.5.9
		E D	D	Display sum-check of fuse data	3.5.9
		E E	--	Edit fuse by number	3.5.10
		--	E	Edit fuse pattern	3.5.10
				Ø Display menu	3.5.10
				#(N) Go to fuse (N)	3.5.10
				space Move cursor right	3.5.10
				backspace[b] Move cursor left	3.5.10
				return Display next row	3.5.10
				CTRL Z Exit fuse editor	3.5.10
		E F	F	Display configuration number	3.5.11
		C E	G	Set option attributes	3.5.12
		--	ESC	Exit terminal control before removing adapter	3.5.13
[a]Except with PALASM adapter. [b]CTRL H is the same as backspace.					
PALASM Design Adapter	Development	--	Ø	Display menu	Refer to PALASM Design Adapter Manual
		--	1	Enter family and pinout codes	
		E 2	2	Receive PALASM source	
		E 3	3	Transmit PALASM source	
		E 4	4	Assemble PALASM source	
		E 5	5	Simulate function table	
	Edit	--	9	Edit source	
		--		Ø Display menu	
		--		B Display line 1	
		--		C Change text	
		--		D Delete character	
		--		E Display to end	
		--		I Insert/enter text	
		--		K Delete current line	
		--		L Display 24 lines	
		--		R(M)(N) Repeat M lines after N	
		--		U Display previous line	
		--		# (N) Go to line N	
		--		space bar Move cursor/prompt right	
		--		back space[b] Move cursor/prompt left	
		--		return Display next line	
		--		DEL/RUB Delete characters (I mode)	
		--		CTRL P Purge all text	
		--		CTRL Z Exit editor, C or I mode	
		--	ESC	Exit terminal control before removing adapter	
[b]CTRL H is the same as backspace.					

(Continued)

Table 3-1. PLDS Command Summary (Cont.)

MODULE OR ADAPTER	COMMAND TYPE	FROM FRONT PANEL	VIA TERMINAL	COMMAND DESCRIPTION	SEE SECTION
H&L Design Adapter	Development	--	0	Display menu	Refer to H&L Design Adapter Manual
		--	1	Enter family and pinout codes	
		E 2	2	Receive data (IFL format)[c]	
		E 3	3	Transmit data (IFL format)	
	Edit	--	4	Edit mode	
		--		G Enter gate number	
		--		P Enter product term number	
		--		T Enter transition term number	
		--		V Move cursor forward	
		--		V Move cursor backward	
		--		F Display next term	
		--		R Display last term	
		--		N Enter next field	
		--		I Insert term	
		--		D Delete term	
		--		C Clear term	
		--		X Deactivate term	
		--		E Display edit sub-menu	
		--		0 Exit edit mode	
		--		1 Return to edit mode	
		--		2 Serial input (receive IFL format)[c]	
		--		3 Serial output (transmit IFL format)	
		--		4 List low-order terms	
		--		5 List high-order terms	
		--		6 Compress terms	
		--		CTRL Z Exit edit mode	
[c]Integrated fuse logic, Signetics ASCII		--	ESC	Exit terminal control before removing adapter	
All P/T Adapters	Device	--	1	Enter family code and pinout code	3.4.1
		Load	2	Load fuse data from device to RAM	3.4.4
		Verify	3	Verify fuse data and perform functional test	3.4.6
		Program	4	Program device with RAM data	3.4.5

NOTE: ESC (escape) returns control to programmer front panel.

3.2 POWER UP

NOTE

If the LogicPak™ with an adapter installed is not in the programmer before power is turned on, you will hear a beep until the LogicPak™ is installed.

When power is applied, the programmer will perform an automatic self-test routine (see subsection 1.4.3 of the LogicPak™ manual). When the self-test routine is complete, the programmer will signal its readiness (see your programmer manual).

To turn the programmer on:

1. Check to make sure a device is not in the socket. If a device is in the socket, lift up the lever (on the upper left of the socket; see subsection 3.4.3), then gently lift the device out of the socket.
2. Plug the AC power cord into the power outlet.
3. Lift the power switch up to the *ON* position (see figure 3-2).

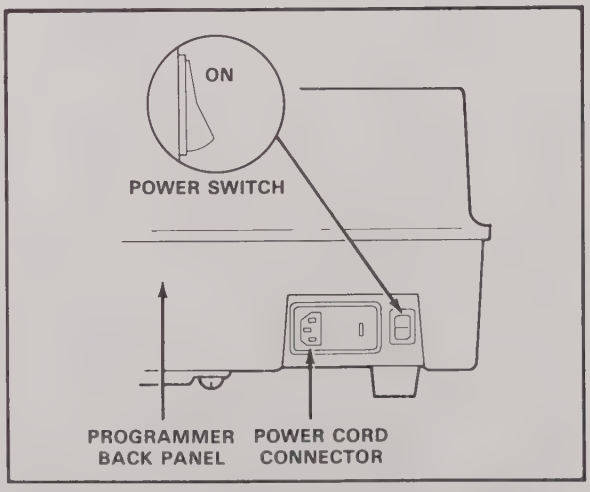


Figure 3-2. Programmer Power Switch Location

3.3 POWER DOWN

CAUTION

Do not turn the power off when a device is in the socket; voltage transients may damage the device.

To turn the programmer power off:

1. Check to make sure the programmer is not in an operation process. If it is, wait until the operation is complete.
2. Check to make sure a device is not in the socket. If a device is in the socket, remove it as described in subsection 3.4.3.
3. Push the power switch down to the *OFF* position (figure 3-2).

3.4 BASIC DATA TRANSFER OPERATIONS

The basic operations that can be accomplished with the LogicPak™ and the Model 29 Universal Programmer are:

- develop data (described in subsection 1.4.1 of the LogicPak™ manual and design adapter manuals),
- load RAM with master device data (described in subsection 3.4.4),
- program a device with RAM data (described in subsection 3.4.5),
- verify RAM data against the device data (described in subsection 3.4.6),
- functionally test device (described in subsection 3.5.7).

The following subsections describe device-related operations with the PLDS using a P/T adapter. Most setup procedures specify that you enter the family and pinout codes because Data I/O recommends that you develop the habit of entering these codes when prompted by the equipment.

If the programmer has been used to program PROMs, or contains data in RAM for some other reason, the fuse pattern developed for logic devices could be adversely affected or option parameters could be inadvertently set. Therefore, execute the "clear RAM" select function (see programmer manual).

All data transfer or verification operations occur between the programmer's internal RAM and the device or between the RAM and serial port in your programmer. Because the operation procedure to transfer data via a serial port varies among programmers, this manual describes only data transfer using the Model 29. For other programmers, refer to the specific programmer operation manual.

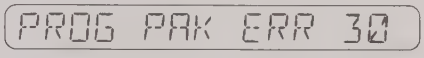
NOTE

An adapter must be installed in the LogicPak™ before any of these operations can be performed (see subsection 2.2).

During copy and verify operations, ADDR *and* SIZE *appear in the Model 29 prompts. These correspond to starting address and block size, respectively. These block limits must remain in the default state for logic device programming. An error code (see section 4, table 4-2) will be displayed if these limits are altered. For more detail on these parameters, see your programmer manual.*

3.4.1 FAMILY CODE AND PINOUT CODE SELECTION

Any device that can be programmed with the LogicPak™ is specified by a unique combination of a two-digit family code and a two-digit pinout code; these codes are provided in appendix A of this manual. Once the codes are entered for a particular device, the LogicPak™ remains set up for any operation with that device until you enter new codes. If invalid family and pinout codes are entered, a beep will sound. In remote control operation,



will be displayed, and the operation will be stopped when you attempt a device operation.

To select the family code and pinout code:

1. Locate the manufacturer name and part number stamped on the device.
2. Go to the family code and pinout code table in appendix A and find the manufacturer's name.
3. Go to the column entitled "Device" and find the number corresponding to the number on the device.
4. Go to the columns labeled "Family" and "Pinout" to find the code numbers corresponding to the device number for the manufacturer of the device.
5. Enter the family code and pinout code you selected from this table when prompted by the programmer or terminal. An LED (light emitting diode) will light above the socket on the adapter.

3.4.2 DEVICE INSERTION

Once you have entered the appropriate family and pinout codes, the LogicPak™ with a P/T adapter installed is ready to accept a device in the socket below the lighted LED.

To install a device:

1. Check to make sure the programmer is not doing an operation. If it is, wait until the operation is complete.
2. Lift the lever on the upper-left side of the socket below the lighted LED (see figure 3-3); the lever will stay in the upright position.
3. Gently set the device in the socket below the lighted LED. Make sure pin 1 of the device is aligned with pin 1 of the socket (upper-left corner); see figure 3-3.
4. A good electrical connection between the device and the socket is essential. To ensure a good connection, push the lever down to lock the device in the socket.

3.4.3 DEVICE REMOVAL

To remove a device:

1. Check to make sure the programmer is not doing an operation. If it is, wait until the operation is complete.
2. Lift the lever on the left side of the socket; see figure 3-3. The lever will remain in the upright position.
3. Lift the device out of the socket; the LED will remain illuminated.

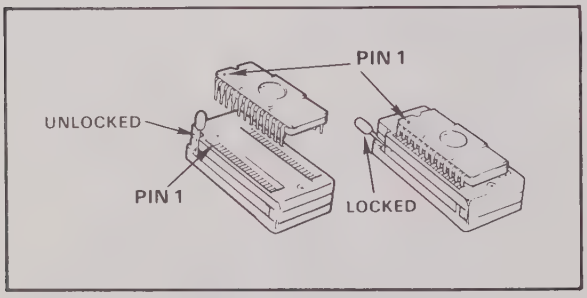


Figure 3-3. Device Installation

3.4.4 LOAD RAM WITH MASTER DEVICE DATA

Front Panel Control

To load the Model 29 RAM with data from a master device with control from programmer front panel, follow the steps given below.

NOTE

If options are desired (see subsection 3.5), select options and parameters as needed before proceeding.

1.

to select the mode.

Model 29 Displays

2.

to select the source of the data.

Model 29 Displays

ADDR/SIZE pertains to block limit parameters. These are PROM related and are not to be used with logic devices. Leave defaults in effect.

3.

to select the destination for the data.

Model 29 Displays

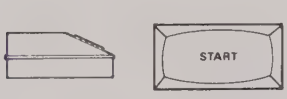
4.

Model 29 Displays

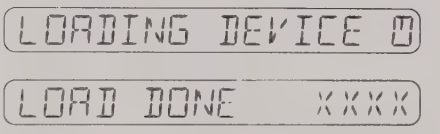
5. Enter the family code and pinout code (see subsection 3.4.1).

NOTE
The socket LED will light.

6. Insert the master device into the appropriate P/T adapter socket. (See subsection 3.4.2.)

7. 

Model 29 Displays



NOTE
XXXX *is the sum-check of the device fuses.*

8. Remove the master device from the adapter socket. (See subsection 3.4.3.)

Fuse data may also be downloaded from a peripheral via the programmer serial port. (Refer to subsection 3.5.9 for instructions.)

Terminal Control

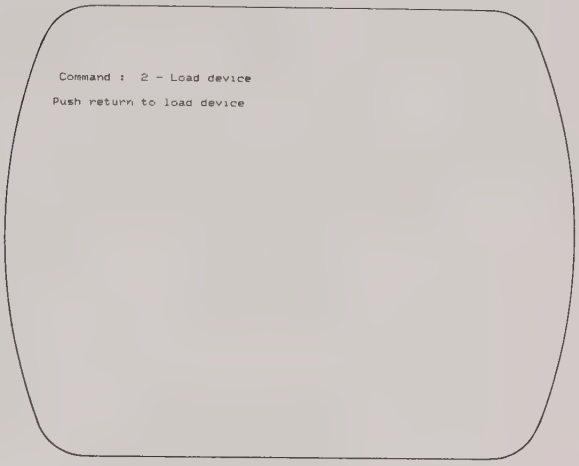
To load the Model 29 with data from a master device using the terminal control mode, follow the steps given below.

1. Place the system in terminal mode; see subsection 3.5.1.
2. Enter the family code and pinout code at the terminal, if prompted by the terminal display.

NOTE
If options are desired (see subsection 3.5), select options and parameters as needed before proceeding.

3.

Terminal Displays



4. Insert master device into socket (see subsection 3.4.2).

5.

Terminal Displays

An action symbol will be displayed while the device is being loaded. When loading is complete, the terminal will display sum-check *XXXX*.

6. Remove device (see subsection 3.4.3).

3.4.5 PROGRAM DEVICE WITH RAM DATA

NOTE

If options are desired (see subsection 3.5), select options and parameters as needed before proceeding.

When programming a device, the system performs illegal-bit tests and blank checks at nominal V_{CC}.

Front Panel Control

To program a blank device with the data in the Model 29 RAM with control from the programmer front panel, follow the steps given below.

1.

Model 29 Displays

2.

Model 29 Displays

3.

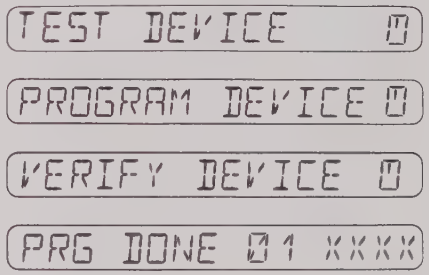
Model 29 Displays

4.

Model 29 Displays

5. Enter the family code and pinout code if required (see subsection 3.4.1).
6. Insert the blank device into the adapter socket (subsection 3.4.2).
7.

Model 29 Displays



sequence number (increments by 1 for each device programmed)

sum-check

8. Remove the device from the adapter socket (see subsection 3.4.3).

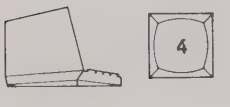
Terminal Remote Control

To program a device with Model 29 RAM data from the terminal control mode:

1. Place the system in the terminal mode (see subsection 3.5.1).
2. Enter the family code and pinout code, if prompted by the terminal.

NOTE

If options are desired (see subsection 3.5), select options and parameters as needed before proceeding.

3. 

Terminal Displays

4. Insert the blank device into the adapter socket (see subsection 3.4.2).

5.

Terminal Displays

An action symbol will be displayed showing the pretesting, programming and verifying of the part. If no errors occur, the terminal displays sum-check *XXXX*.

NOTE

XXXX *is the sum-check of the device fuses.*

6. Remove the device from the adapter socket (see subsection 3.4.3).

3.4.6 VERIFY AND FUNCTIONALLY TEST DEVICE

Front Panel Control

The verify routine compares the device data to RAM data and performs functional testing, if this option is selected (see subsection 3.5.5).

To verify and functionally test a device from Model 29 front panel control, perform the following steps:

NOTE

If options are desired (see subsection 3.5), select options and parameters as needed before proceeding.

1.

   Model 29 Displays

   VERIFY DATA FROM

2.

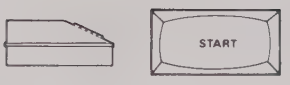
   Model 29 Displays

   DEV, ADDR/SIZE TO

3.

   Model 29 Displays

   VE DEV) RAM, ADDR

4. 

   Model 29 Displays

   FAM, 00 PIN 00

5. Enter the family code and pinout code if required (see subsection 3.4.1).
6. Insert the device to be verified and/or tested into the adapter socket (see subsection 3.4.2).
7.

   Model 29 Displays

   VERIFY DEVICE 0

   VE DEV DONE XXXX

   NOTE

   XXXX *is the sum-check of the device fuses.*

8. Remove the master device from the adapter socket (see subsection 3.4.3).

Terminal Control

To verify and test a device from terminal control, follow the steps given below.

1. Place the system in the terminal mode; see subsection 3.5.1.
2. Enter the family code and pinout code, if prompted by the terminal.

   NOTE

   If options are desired (see subsection 3.5), select options and parameters as needed before proceeding.

3. Insert device to be verified (see subsection 3.4.2).
4.

   Terminal Displays

An action symbol will be displayed showing the verification function under way. Upon completion the terminal will display sum-check *XXXX* of the device fuses.

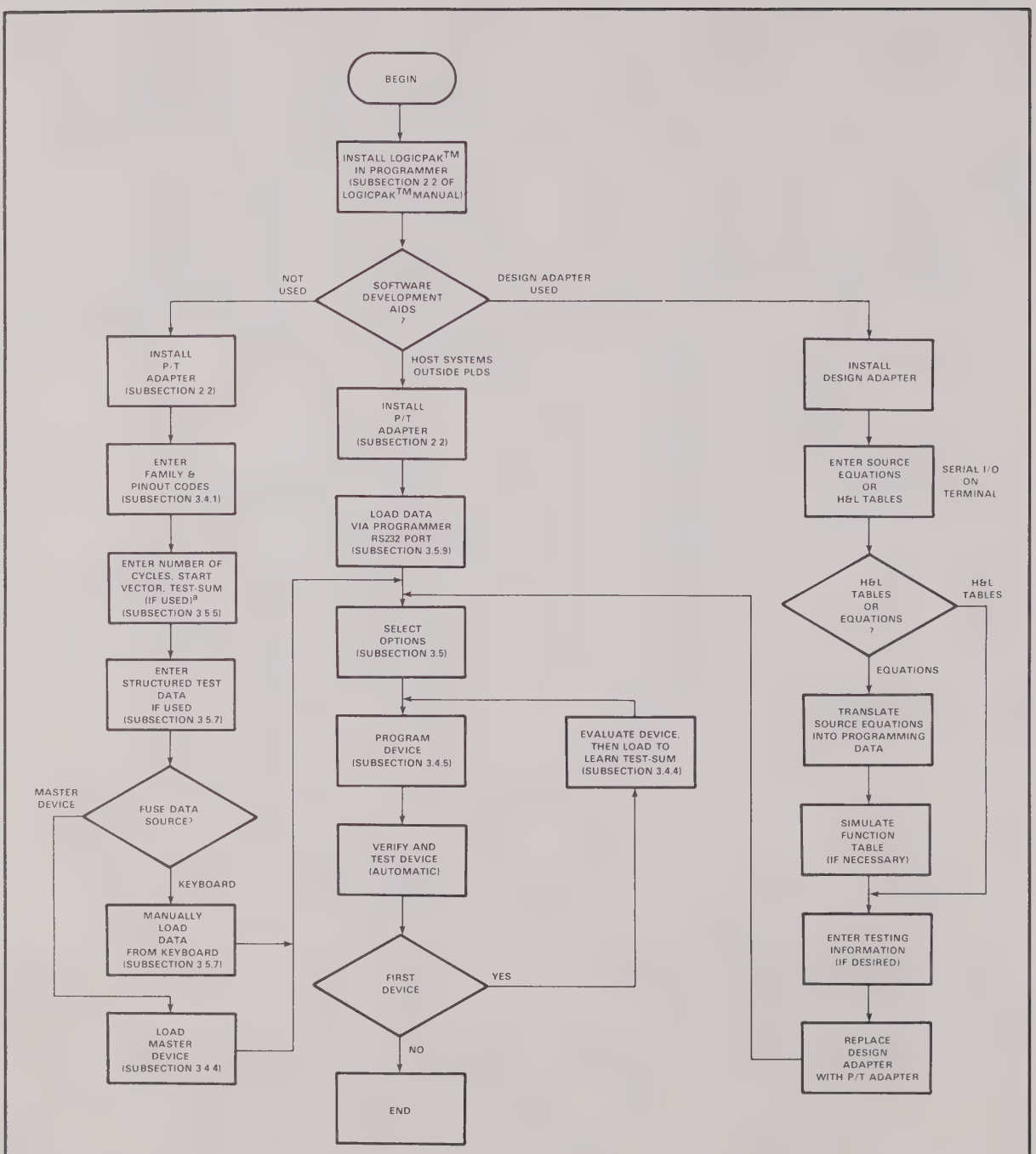
5. Remove device from the adapter socket (see subsection 3.4.3).

3.5 SYSTEM COMMANDS

In addition to the copy (load or program), verify, edit, and select functions described in the Operation section of your programmer manual, the LogicPak™ offers numerous system commands that allow you to manipulate data and set parameters. System commands are accessed by entering a two-character select code from the programmer front panel or a one-character menu code from the terminal. Some commands will prompt for data entry. The operational overview (figure 3-4) will help you develop data and program a device using the system commands and programmer operations. Table 3-1 lists the select codes for Data I/O programmers to enter system commands from the programmer front panel and the menu codes for control from a terminal in terminal mode.

NOTE

The sequence explanations assume no operating errors. If these occur, the programmer signals with a beep and displays a two-digit error code in front panel mode or an error message in terminal mode. It also beeps once when an incorrect key is pressed. Error codes are explained in subsection 4.1 (table 4-2) and in your programmer manual. Some errors will return you to the programmer front panel control from the terminal mode.


BEGIN
INSTALL LOGICPAK™ IN PROGRAMMER (SUBSECTION 2.2 OF LOGICPAK™ MANUAL)
SOFTWARE DEVELOPMENT AIDS ?
NOT USED
DESIGN ADAPTER USED
HOST SYSTEMS OUTSIDE PLDS
INSTALL P-T ADAPTER (SUBSECTION 2.2)
ENTER FAMILY & PINOUT CODES (SUBSECTION 3.4.1)
ENTER NUMBER OF CYCLES, START VECTOR, TEST-SUM (IF USED)[a] (SUBSECTION 3.5.5)
ENTER STRUCTURED TEST DATA IF USED (SUBSECTION 3.5.7)
FUSE DATA SOURCE?
MASTER DEVICE
KEYBOARD
MANUALLY LOAD DATA FROM KEYBOARD (SUBSECTION 3.5.7)
LOAD MASTER DEVICE (SUBSECTION 3.4.4)
INSTALL P/T ADAPTER (SUBSECTION 2.2)
LOAD DATA VIA PROGRAMMER RS232 PORT (SUBSECTION 3.5.9)
SELECT OPTIONS (SUBSECTION 3.5)
PROGRAM DEVICE (SUBSECTION 3.4.5)
EVALUATE DEVICE, THEN LOAD TO LEARN TEST-SUM (SUBSECTION 3.4.4)
VERIFY AND TEST DEVICE (AUTOMATIC)
FIRST DEVICE
YES
NO
END
INSTALL DESIGN ADAPTER
ENTER SOURCE EQUATIONS OR H&L TABLES
SERIAL I/O ON TERMINAL
H&L TABLES OR EQUATIONS ?
H&L TABLES
EQUATIONS
TRANSLATE SOURCE EQUATIONS INTO PROGRAMMING DATA
SIMULATE FUNCTION TABLE (IF NECESSARY)
ENTER TESTING INFORMATION (IF DESIRED)
REPLACE DESIGN ADAPTER WITH P/T ADAPTER

(a) Logic Fingerprint™ test sum may also be derived from the master device (see section 1.4 of the LogicPak™ manual).

Figure 3-4. Operational Overview Flowchart

3.5.1 ENABLE TERMINAL MODE

Select code *E1* transfers control of the PLDS to the terminal. After control is transferred, the Model 29 will display only its action symbol. This command allows you to access data development and remote operations resident in the design adapters and remote operations using the P/T adapters.

The terminal will prompt you to enter family codes and pinout codes unless they have already been entered. For P/T adapters only, see subsection 3.5.3. The terminal will then display the command menu (see figure 3-5).

See subsection 2.6 of the LogicPak™ manual for terminal setup procedure.

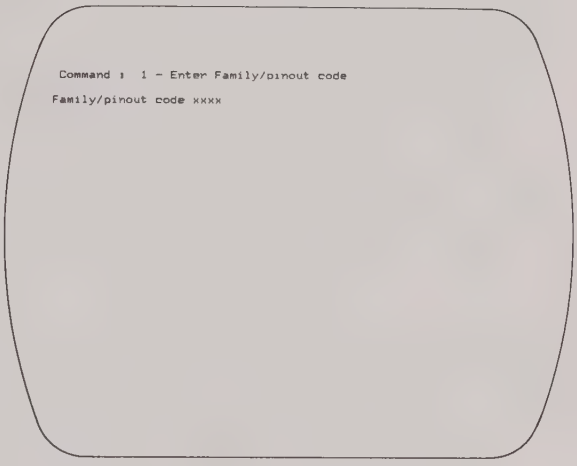
3.5.2 DISPLAY COMMAND MENU

This command causes the PLDS to redisplay its command menu on the terminal, as shown in figure 3-5.

3.5.3 FAMILY CODE AND PINOUT CODE

From the Model 29 front panel control, family code and pinout code entry is part of device-related operations (see subsections 3.4.1 through 3.4.5).

Terminal Displays



Enter the family code and pinout code (see subsection 3.4.1 for more detail). Space and backspace *(CTRL H)* may be used to move the cursor back and forth.

```
Command :  0 - Display menu

DATA I/O CORP. - Programmable Logic Development System - 303A-V04
                    Copyright 1982,1983,1984

      - GENERAL COMMANDS -                    - I/O COMMANDS -
0 - Display menu                        B - Receive JEDEC data
1 - Enter Family/pinout code            C - Transmit JEDEC data
5 - Enter reject count option
6 - Enter verify option
7 - Enter security fuse option
8 - Enter functional test data
F - Configuration number
G - Select attributes

    - DEVICE RELATED COMMANDS -             - FUSE MAP COMMANDS -
2 - Load device                         A - Display fuse pattern
3 - Verify device                       D - Display fuse sumcheck
4 - Program device                      E - Edit fuse pattern

NOTE - Always transmit an "ESC" before removing adapter
```

Figure 3-5. PLDS Command Menu

3.5.4 SET REJECT COUNT OPTION

This command allows you to select the number of programming pulses applied to the device fuses before the programmer rejects the device as unprogrammable. The default value of Ø selects the manufacturer's specified number of programming pulses. Refer to the timing diagrams in section 4 for specific entries to select optional reject values.

NOTE

The PALASM adapter does not provide this option.

Front Panel Operation

Model 29 Displays

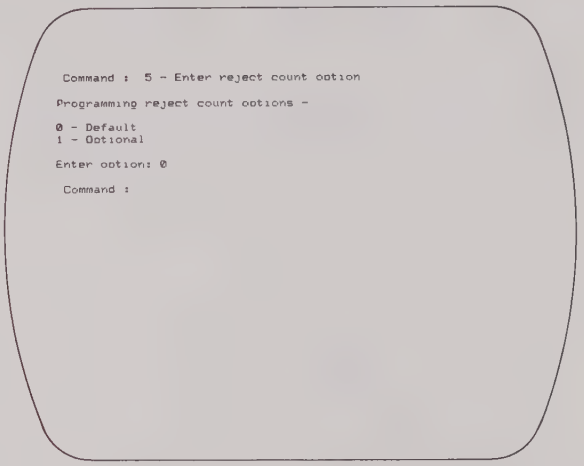
To change the reject count to an optional value, enter the code number *(X)* specified in the timing diagrams in section 4.

Model 29 Displays

Terminal Operation

To select the reject count from the terminal, enter a 5 from the command mode, then respond to the prompt with the code number.

Terminal Displays



3.5.5 SELECT VERIFY OPTION

Three options are available for selecting verify and functional test routines. These routines are described in detail in subsection 3.4.6.

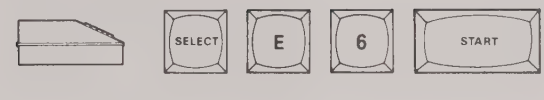
Options available are:

OPTIONS	DESCRIPTION
	Default option. Perform fuse verify, followed by structured test (if test vectors are present in RAM), and Logic Fingerprint™ test (if one or more Logic Fingerprint™ test cycles are selected), in that order.
	Perform fuse verify only.
	Perform structured test and Logic Fingerprint™ test only, in that order. Do not perform fuse verify.

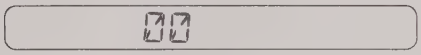
Option Ø (default) is the option used in normal operation. Option 1 checks the programming of the device fuses without checking device functionality. Use option 2 to functionally test devices with the security fuse blown. In addition, option 2 can be used to learn the Logic Fingerprint™ test of a device with the security fuse blown. Fuse data in RAM will be cleared during this operation. Programming cannot occur with option 2 selected.

Verify options must be entered from either the programmer's keyboard or a terminal. The option will remain in effect until it is changed or until the unit is powered down. To reselect the default, key in option Ø.

Front Panel Operation

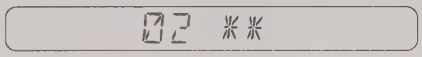


Model 29 Displays



At this point, to select functional test, for example, do the steps which follow.

Model 29 Displays



Terminal Operation

To enter the verify option from the terminal, enter 6 from the command mode, then respond to the prompt with the desired option. For example, to select functional test:

Terminal Displays

Command : 6 - Enter verify option
0 - Sequence - fuse verify, structured test, Logic Fingerprint
1 - Fuse verify only
2 - Sequence - structured test, Logic Fingerprint
Enter verify option: 2
Command :

3.5.6 SELECT SECURITY FUSE OPTION

Some logic devices are equipped with protective fuses called security fuses. Once the security fuses are programmed, the fuse states in the logic array cannot be copied. Programming the security fuses makes it very difficult to pirate a device design.

The PLDS security fuse programming feature is a fail-safe function. You can either enable programming of the security fuse at all times, allow programming only when security fuse data are downloaded to the PLDS via the serial port, or disable programming completely, whether security fuse data are downloaded or not.

When the security fuse has been blown, a Logic Fingerprint™ test and structured test can still be performed, but a fuse verify operation is not possible (see subsubsection 3.5.5). When programming the security fuse on MMI registered PAL®s, be aware that the device registers will auto-preset to a different state after the security fuse is blown. This will result in a different Logic Fingerprint™ test sum than the one "learned" from a master device with the security fuse intact. (Refer to subsection 3.6 for more information.)

To enable programming of security fuses, two conditions must be met: 1) the security fuse state in the programmer RAM must be 1 (or true), and 2) security fuse programming must be enabled. Once the security fuse option is selected, it will remain in effect until changed or until the programmer is turned off.

When security fuse data are entered into RAM in the JEDEC ASCII-logic format, data in the **G** field indicate the state of the security fuse. The **G** field does not affect the enable state of the security fuse option; the enable state must be entered separately. This can be done before or after loading JEDEC ASCII-logic format data.

Security fuse states cannot be loaded from a master device.

CAUTION

Once the security fuse is blown, you no longer can verify the state of any fuse in the device. The process cannot be reversed; therefore, be certain that you want to program the security fuse before you activate this function. Attempting to reprogram the device after the security fuse is blown will alter the original fuse pattern and render the device inoperative.

Front Panel Operation

To select a security fuse option from the front panel:

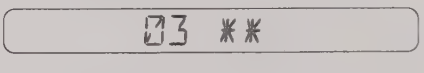
Model 29 Displays

Security fuse select-code options are:

OPTION	DESCRIPTION
0	Default option. Disable programming and set the security fuse state in RAM to Ø (unprogrammed).
1	Disable programming, and set security fuse state in RAM to 1 (programmed).
2	Enable programming, and set security fuse state in RAM to Ø. (Data downloaded in the JEDEC format can change the security fuse state to 1.)
3	Enable programming, and set security fuse state in RAM to 1. (Data downloaded in the JEDEC format can change the security fuse bit back to Ø.)

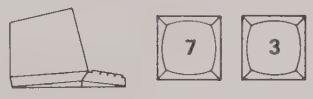
For example, to enable security fuse programming and set security fuse state in RAM to 1 (option 3):

Model 29 Displays



Terminal Operation

To enter the security fuse option from the terminal, enter 7 from the command mode, then respond to the prompt with the desired option. For example, to enable security fuse programming and set security fuse state in RAM to 1, do the following:



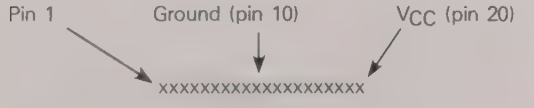
Terminal Displays

```
Command : 7 - Enter security fuse option

          SECURITY      SECURITY FUSE
OPTION    FUSE DATA      PROGRAMMING

   0 -------- 0 -------- disabled
   1 -------- 1 -------- disabled
   2 -------- 0 -------- enabled
   3 -------- 1 -------- enabled

Enter Security Fuse option: 3

Command :
```

3.5.7 ENTER FUNCTIONAL TEST DATA

Functional test data includes information for the Logic Fingerprint™ test and also the test vectors used by P/T adapters for testing of a programmed device. The Logic Fingerprint™ test information consists of three components:

- The number of test cycles to be performed during the Logic Fingerprint™ test (described later in this subsection). The default value is ØØ, which disables the Logic Fingerprint™ test.
- The Logic Fingerprint™ starting vector. This is an arbitrary binary sequence, each bit of which corresponds to a pin on the device under test. The starting vector format for a 20-pin device is shown below. Each "x" represents a "1" or a "0" to apply a logic high or logic low to the corresponding pin. Values entered for V_{CC} and ground affect the resulting Logic Fingerprint™ test signature, but have no effect on the device under test.



The starting vector is used to initialize the Logic Fingerprint™, and is one of the components (along with the device type, number of test cycles, and programming pattern) which determine the resulting Logic Fingerprint™ test signature. Note that different Logic Fingerprint™ test signatures may result for a given logic design, depending on the choice of starting vector.

- The Logic Fingerprint™ test signature itself is the result of performing the Logic Fingerprint™ test, as described later in this subsection.

Logic Fingerprint™ test data may be entered from either the front panel or the terminal. From the front panel, the number of test cycles and the starting vector for the Logic Fingerprint™ test may be entered, and the resulting Logic Fingerprint™ test signature may be viewed or entered. Structured test vectors may not be entered or edited from the front panel but only from a terminal or serial download. All functional test data may be entered from the terminal, including number of test cycles, starting vector, the Logic Fingerprint™ test signature itself, and the test vectors.

NOTE

If a value is entered for the Logic Fingerprint™ test signature, it should be either ØØØØØØØØ or a known-good value corresponding to the number of test cycles, starting vector, device, and fuse patterns under test. A value of ØØØØØØØØ will cause the LogicPak™ to "learn" the correct Logic Fingerprint™ test signature when a Load, Program, or Verify operation is performed (see subsection 3.4 for details). When in Load, the correct Logic Fingerprint™ will be learned independently of the value entered.

If "Device Selection Error" (Error 30) appears when you select functional test data, you must specify family code and pinout code to define the vector width.

In the subsections which follow, functional test data will be entered to test the Basic Gates design example[a].

Front Panel Operation

From the front panel, the number of test cycles and the Logic Fingerprint™ starting vector may be entered, and the Logic Fingerprint™ test signature may be viewed or entered.

Set Number of Logic Fingerprint™ Test Cycles.

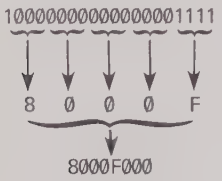
Model 29 Displays

For example, to enable one cycle of testing,

Model 29 Displays

Logic Fingerprint™ and Starting Vector

The starting vector must be converted from the binary form to hexadecimal for entry from the front panel. For our Basic Gates example, we will choose an arbitrary test vector as shown:



Starting vector (binary)

(hexadecimal)

Starting vector (hexadecimal)

The unused portion of the 32-bit vector is assumed to be zeroes and must be included in the hexadecimal vector entry.

For example:

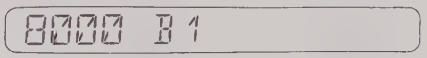
Model 29 Displays

NOTE

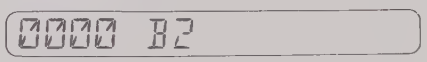
The eight-character starting vector is entered into the programmer in two fields. B1 *identifies the first field.*

To enter the first four hexadecimal digits,

Model 29 Displays



Model 29 Displays



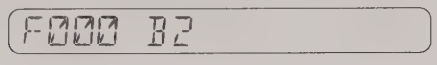
NOTE

B2 *represents the second field.*

[a]Adapted from THE MMI PAL HANDBOOK, available from Monolithic Memories, Inc., 1165 Arques Avenue, Sunnyvale, California 94086.

Enter the remaining hexadecimal digit by pressing

Model 29 Displays

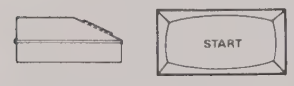


The zeroes are ignored, but are needed to correctly position the "F."

This vector, when applied to the Basic Gates example, produces the Logic Fingerprint™ test signature:

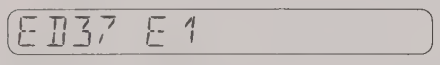
ED37A9E4 (hexadecimal)

This value may be viewed or entered at this time by pressing *START:*

1. 

Enter the first four characters of the Logic Fingerprint™ test signature if desired.

Model 29 Displays

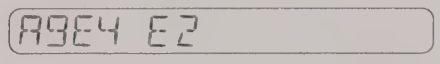


The first four characters are displayed as the *E1* field. The last four characters (*E2* field) may be viewed or entered by pressing *START* again:

2.

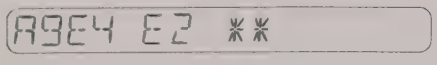
Enter the next four characters if desired.

Model 29 Displays



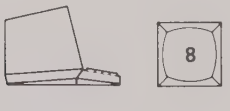
3.

Model 29 Displays



Terminal Operation

Entering an "8" from the Command mode allows you to enter functional test data and begin vector editing from the terminal.



The functional test data may be entered in response to three prompts (see figure 3-6).

```
Command : 8 - Enter functional test data

Cycles for Fingerprint: xx
Fingerprint starting vector: xxxxxxxxxxxxxxxxxxx
Fingerprint: xxxxxxxx
```

Note: x represents current values

- **Figure 3-6. Prompts for Entering Functional Test Data**

As each prompt appears, you may modify the current values (represented by x's in figure 3-6) using the following steps:

1. Move the cursor forward (using the spacebar) and backward (using the backspace) along the displayed value until it is positioned over the symbol to be changed.
2. Press the desired symbol.
3. Enter *RETURN* at any point to move to the next prompt.
4. *CTRL Z* is used to exit the functional test data entry mode.

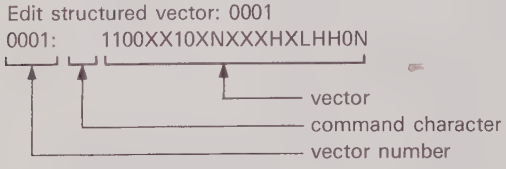
For our test example, the values shown in figure 3-7 should be entered.

Vector Editing

Vectors are created by downloading JEDEC 'V' fields, simulating a source file containing a function table, or by using the vector editor.

When the Logic Fingerprint™ test information has been entered (or skipped by entering *RETURN*), the vector editor menu appears (see figure 3-7), and a prompt appears for the vector number to be edited. The default vector is 0001, as shown in figure 3-7.

The vector editor is a fixed-format line editor with the first column of the displayed line reserved for command characters, as shown below.



A character entered in the first column (normally blank) is interpreted as a command and acted upon immediately; otherwise, vector editing is not processed until a *RETURN* is entered (at any point on the line). The command characters recognized in the first column are Ø, U, #, D, and R; see table 3-2 for command character definitions.

During operation, the vector editor copies the selected vector to a temporary buffer where all editing changes are made. Then, when a *RETURN* command is entered, the temporary buffer is examined for legal characters before copying back to vector memory. You are not allowed to proceed to another vector until all characters are legal in the current vector. Typing a *CTRL Z* to exit the vector editor will leave the selected vector in its original state.

An "empty vector" is represented by a dash in all pin positions. This will appear as the first vector in an empty vector editor buffer, or as one past the last vector where data are present in memory. All vectors are numbered lower than the empty vector.

Table 3-2. Vector Editor Command Characters

COMMAND	DESCRIPTION	ACTIVITY
0 (zero)	Display menu	Redisplays menu and restarts editing on the same vector.
U	Up (previous vector)	Moves editing to the next lower vector number (the vector one 'up' on the screen).
#(N)	Go to vector (N)	Entering a '#' in the command column causes the vector editor to prompt for the desired vector number (default = 0001). Entering a vector number greater than the last vector will move you to the last vector.
D	Delete current vector	Current vector is deleted, and all higher vectors moved down one. Current vector number is redisplayed with new vector.
R	Repeat current vector	Creates a copy of the current vector immediately following the current vector. The copy is displayed, with its vector number (one greater than the original). This command may be given for any vector, and existing vectors will be moved to accommodate the new copy.

```
Command :  8 - Enter functional test data
Cycles for Fingerprint: 01
Fingerprint starting vector: 10000000000000001111
Fingerprint: ED37A9E4

            - DISPLAY  -                        - EDITING COMMANDS -
0 ------------ Display menu              D ------- Delete (Kill) current vector
Return -------- Go to next vector         R ------- Repeat current vector
U ------------- Up (previous vector)      CTRL Z -- Exit vector editor
#(N) ---------- Go to vector (N)
Space --------- Move cursor right
BKSP (CTRL H) - Move cursor left
CTRL Z -------- Exit vector editor

Edit structured vector:  0000
0001:  1100XX10XNXXXHXLHH0N
0002:  --------------------
```

Figure 3-7. Entering Functional Test Data

To edit a vector, follow the steps below.

1. Move the cursor forward (using the spacebar) and backward (using the backspace) along the displayed vector until it is positioned over the test condition to be changed.
2. Type the desired test symbol to enter it into the vector image; the allowable test conditions are 0-9, X, N, F, H, L, Z, C, P, and K (see table 3-3 for test symbol definition).

Table 3-3. Vector Symbol Definition

VECTOR SYMBOL	DEFINITION
0	Drive input low
1	Drive input high
2-9	Drive input to supervoltage #2-9
C	Drive input low, high, low
K	Drive input high, low, high
N	Power pins and outputs not tested
L	Test output low
H	Test output high
Z	Test output for high impedance
F	Float input or output
X	Ignore input or output (not defined in JEDEC format)
P	Preload (applied to clock pin)

NOTE

"X" is not defined in the JEDEC format. The "X" is treated as an "N" for outputs and leaves an input at its previously defined state.

Test conditions 2 through 9 specify non-TTL levels (supervoltages) that access special device features. A device may be damaged by improper use of supervoltages.

3. Enter *RETURN* or *CTRL Z* at any point to move to the next vector or to exit the vector editor.

Register Preload. In some registered logic devices, the internal registers can be arbitrarily loaded to a desired state. This capability allows easier functional testing by providing a means of achieving states which may be difficult or impossible to enter by normal state transitions.

For devices which have the register preload feature (see table 3-4) preload is accomplished by using a "preload vector," a structured vector which has a "P" symbol in the clock pin position. Also in the preload vector are special symbols in the positions of the pins associated with loading of the registers. The symbols used in the preload vector and their functions are described in table 3-5.

Table 3-4. Preloadable Devices

PAL16RP8	PAL16R8BP
PAL16RP6	PAL20R4BP
PAL16RP4	PAL20R6BP
PAL20RP10	PAL20R8BP
PAL20RP8	PAL20X4A
PAL20RP4	PAL20X8A
PAL16R4BP	PAL20X10A
PAL16R6BP	

Table 3-5. Preload Vector Symbols

P	Identifies preload vector and invokes preload algorithm. (Allowed on clock pin only; otherwise treated as "X".)
Ø	Preloads a logic "Ø" into the register $\overline{Q}$ output, meaning a logic "1" will be loaded into the register Q output. Does not test device outputs.
1	Preloads a logic "1" into the register $\overline{Q}$ output, meaning a logic "Ø" will be loaded into the register Q output. Does not test device outputs.
L	Preloads register with the appropriate level such that a logic "Ø" appears on the device output pin. Also tests the preloaded device output and indicates an error if a logic "Ø" is not found.
H	Preloads register with the appropriate level such that a logic "1" appears on the device output pin. Also tests the preloaded device output and indicates an error if a logic "1" is not found.

All pins not used in the device's preload algorithm (regardless of the symbol placed in the preload vector pin position) are treated as "X"s (left in their previous state). Pins which are used in the preload algorithm may not return to their original state following preload. For example, to preload a 20-pin device with preload pins (most likely device outputs) 12 through 19, you might apply the following preload vector: (clock pin assumed to be pin 1).

0001: PXXXXXXXXNXHLHLHLHLN

When the preload vector is applied during functional testing, the device-specific preload algorithm is invoked and the registers are loaded with the appropriate data to make the outputs high ("H") or low ("L"). The output pins are then tested to verify that the preload was successful.

Assuming the device has an inverter between the register output and the output pin, another method of achieving the same results as above is to use the following two vectors:

0001: PXXXXXXXXNX1Ø1Ø1Ø1ØN
0002: XXXXXXXXXNØHLHLHLHLN

The first vector is a preload vector using "1"s and "Ø"s to load the $\overline{Q}$ output of the register with the data indicated (thus making the Q outputs of the registers the complements of the data in the vector). Since we have assumed an inverter between the Q output and the output pin, the data found on the output pins after execution of the preload vector should reflect the "1"s and "Ø"s in the preload vector. The second vector shown is a conventional structured vector which tests the outputs for the desired data.

The "1" and "Ø" preload symbols are most useful for preloading registers whose state cannot be read at a device pin, or for any case in which the user is concerned with setting up the state of the REGISTERS and not necessarily the state of the output pins.

The "H" and "L" preload symbols are used to preload the states of OUTPUT PINS whose states are determined by the data in internal registers. The programming/testing adapter firmware determines what data should be placed in the internal registers to provide the correct outputs. Users concerned with preloading the state of the internal registers can use the "H/L" preload vector to load and automatically verify internal register states provided that data inversion (if any) between registers and outputs is considered.

3.5.8 DISPLAY FUSE PATTERN

This command transmits the fuse pattern in the programmer data RAM to the serial port. The fuse states may be shown as a series of "1"s and "0"s or a series of "-"s and "X"s; see subsection 3.5.12 on selecting characters. The "1" or "-" represents a high-resistance or "blown" fuse in a fuse link device. The "0" or "X" represents a low-resistance or "intact" fuse. Each fuse can be identified by a decimal fuse number, as shown in figure 3-8. The fuse states are arranged in a matrix that corresponds to the logic diagram of the device (figure 3-9). This is useful for comparing or copying a displayed fuse pattern to the device logic diagram. Logic diagrams for all supported devices are in appendix A.

NOTE

Sending certain control characters to the PLDS during the course of fuse pattern display will affect the display. The output may be stopped by sending a CONTROL S *(DC1 or ASCII, 11 hex) and then restarted by sending a* CONTROL Q *(DC3 or ASCII 13 hex).*

A CONTROL Y *(ASCII, 19 hex) will terminate the transmission and return to the terminal or front panel operation.*

An ESC *(escape) character (ASCII 1B hex) will terminate the transmission and return to front panel operation.*

The last character of the fuse pattern transmission is either *CONTROL C* (*ETX* or ASCII *03*) or a *CONTROL Z* (ASCII *1A* hex). (See subsection 3.5.12 on selecting the termination character.)

```
Command : A - Display fuse pattern

      00          10          20
0000  -------X--   ----------  ----
0024  XXXXXXXXXX  XXXXXXXXXX  XXXX
0048  XXXXXXXXXX  XXXXXXXXXX  XXXX
0072  XXXXXXXXXX  XXXXXXXXXX  XXXX
0096  X-X-------  ----------  ----
0120  XXXXXXXXXX  XXXXXXXXXX  XXXX
0144  ----X-----  ----------  ----
0168  --------X-  ----------  ----
0192  ----------  -X-X------  ----
0216  XXXXXXXXXX  XXXXXXXXXX  XXXX
0240  ----------  ----X--X--  ----
0264  ----------  -----XX---  ----
0288  ----------  ----------  -X--
0312  ----------  ----------  ---X
0336  ----------  ---------X  ----
0360  XXXXXXXXXX  XXXXXXXXXX  XXXX
Sumcheck 1BB9

Command :

NOTE: - = open
      X = intact

Fuse Number = First Fuse Number + Increment
```

Figure 3-8. Complete Fuse Pattern

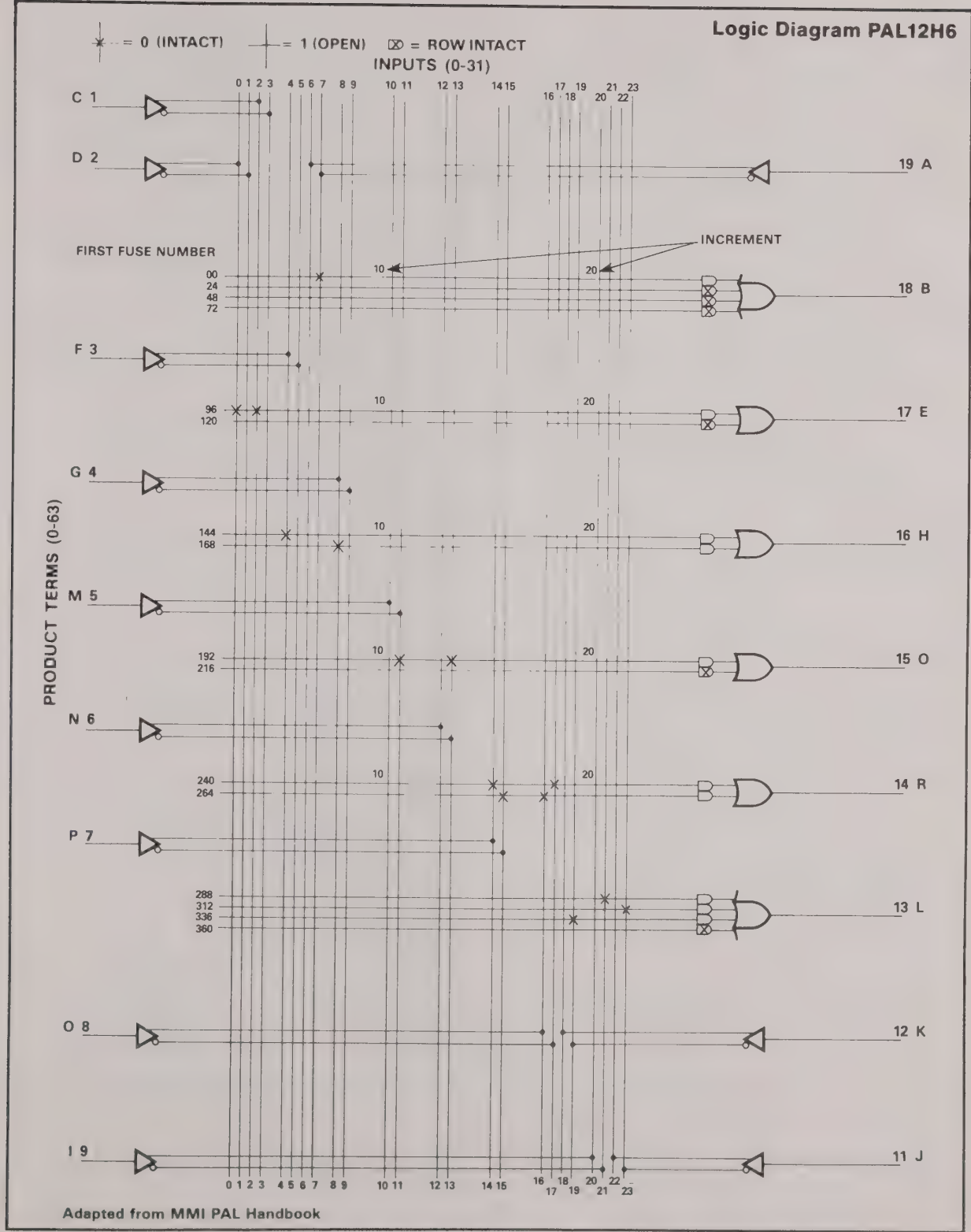
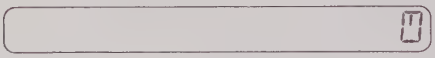


Figure 3-9. Logic Diagram for Basic Gates Example

Front Panel Control

To display the fuse pattern from front panel control, follow these steps:

Model 29 Displays



Model 29 Displays

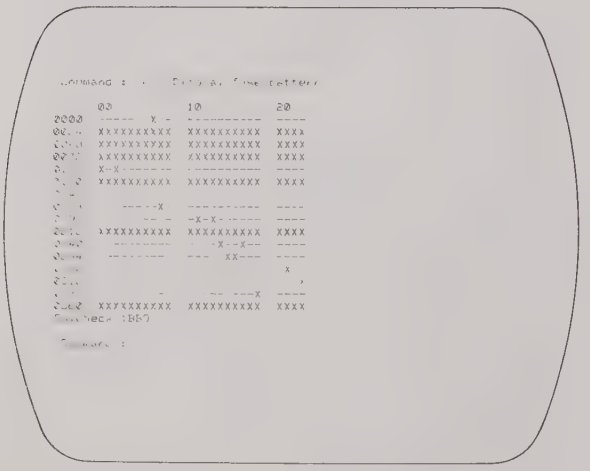
NOTE

↑ is the action symbol. XXXX is the fuse array checksum.

Terminal Control

To display the fuse pattern from the terminal command mode, enter an *A*:

Terminal Displays



3.5.9 JEDEC FORMAT DATA EXCHANGE

Fuse data, test vectors, and the Logic Fingerprint™ test signature are transmitted between the host computer and the PLDS in the JEDEC format. The JEDEC format is described in detail in appendix A of the LogicPak™ manual. A brief overview of the format is provided in this section, and shown in figures 3-10 and 3-11. Figure 3-10 shows an example JEDEC transmission and its components.

The transmission consists of a start-of-text *STX* character, the various fields, an end-of-text *ETX* character, and a transmission checksum, as shown in figure 3-11.

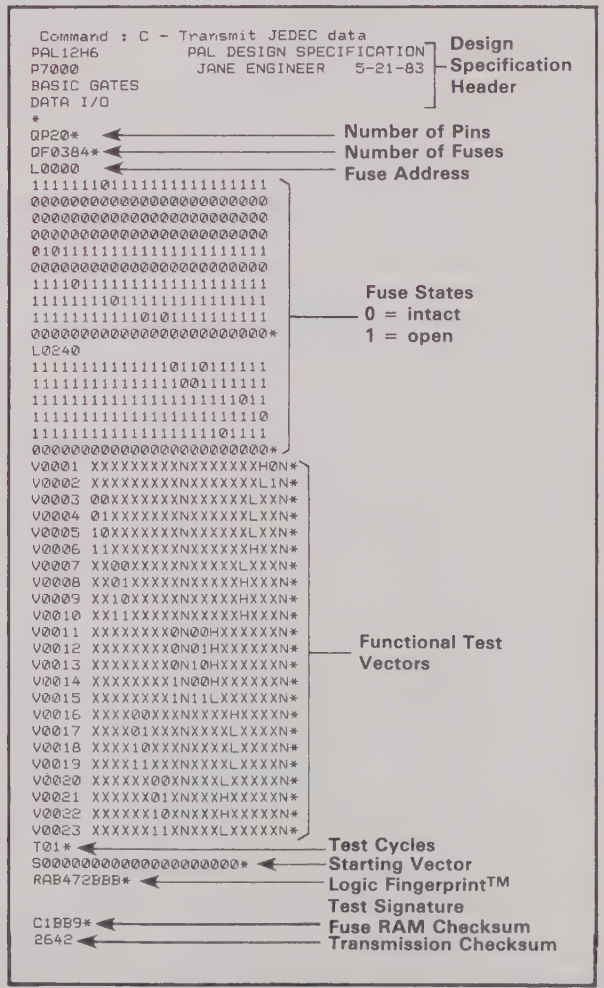


Figure 3-10. JEDEC Transmission—Basic Gates Example

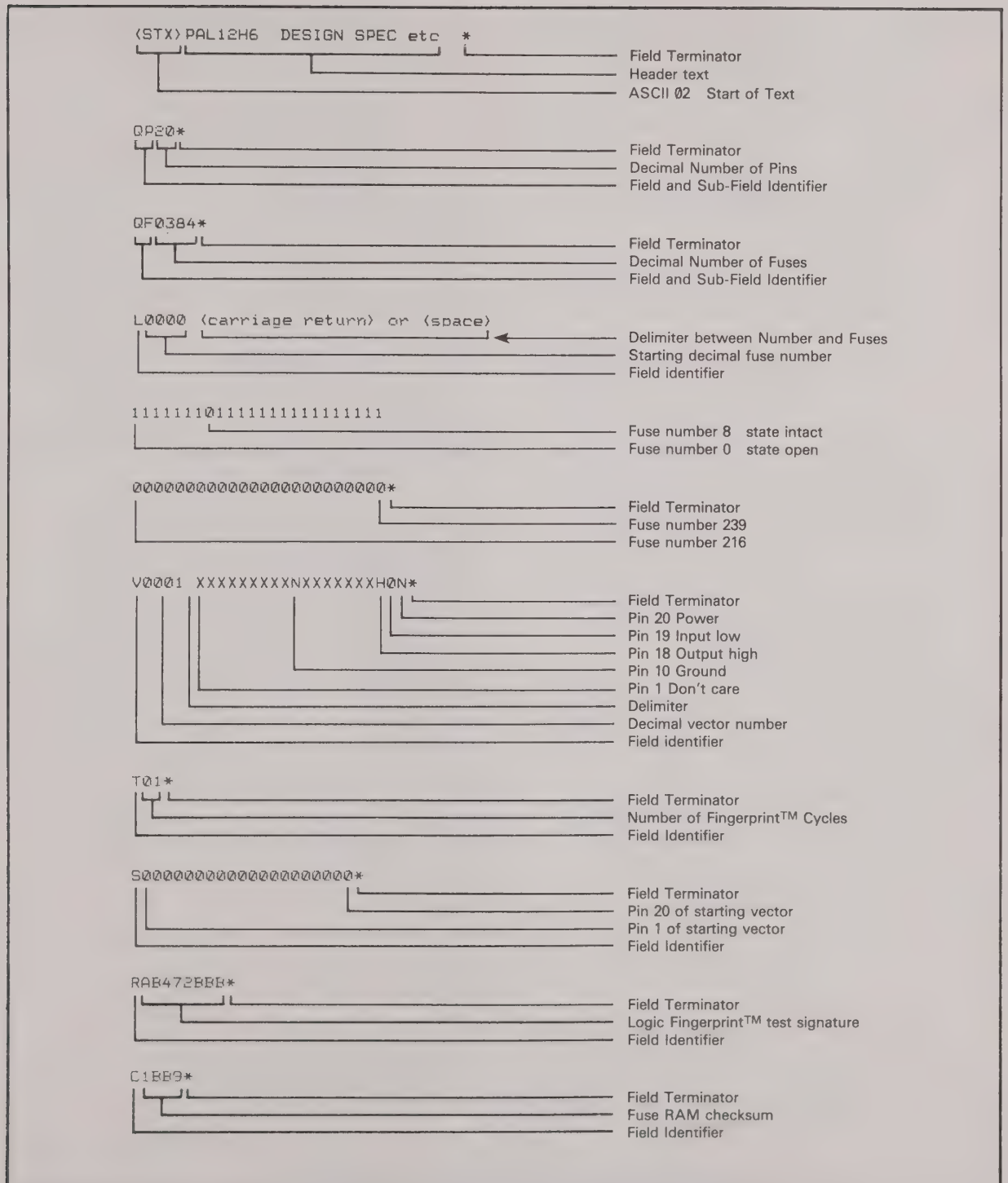


Figure 3-11. JEDEC Format (Breakdown of Figure 3-10) (Continued)

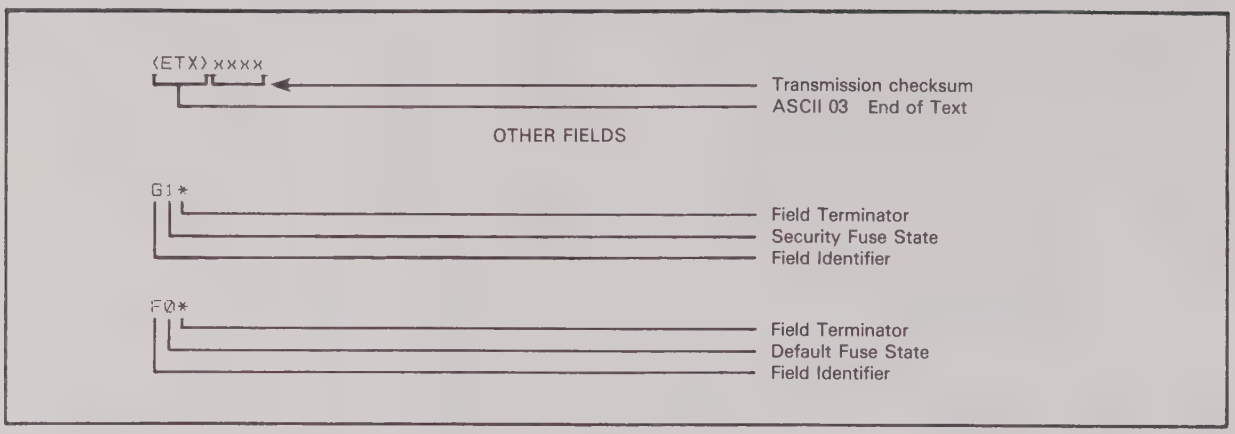


Figure 3-11. JEDEC Format (Breakdown of Figure 3-10) (Cont.)

The transmission checksum is the 16-bit sum of all ASCII characters transmitted between and including the *STX* and *ETX*. The parity bit is excluded in the calculation (see figure 3-12). The transmission checksum computed by the PLDS may be found by examining data RAM addresses 405 and 406, using the programmer's *EDIT* mode (discussed later in this subsection). Some computer operating systems do not allow a user to control what characters are sent, especially at the end of a line. The transmission checksum may be disabled in this case by sending a dummy checksum of *0000*.

In general, each field in the format starts with an identifier, is followed by the information, and is terminated with an asterisk. For example, "T01*" sets the number of Logic Fingerprint™ test cycles to 1. The design specification header does not have an identifier and must be the first field in the transmission, immediately following the *STX*.

Fuse information is specified by the "QF", "F", "L", and "C" fields. The "QF", "F", and "C" fields are optional.

The "QF" field sets the maximum allowable number of fuses. The "F" field sets the default fuse value. An "F0*" fills the fuse RAM with 0s, and an "F1*" fills the fuse RAM with 1s. This operation takes a significant amount of time and can lead to an input buffer overflow at high baud rates.

The "L" field starts with a decimal fuse number and is followed by a stream of fuse states (1 or 0). The fuse number may include leading zeroes (i.e., "L12" and "L0012" are the same). A "space" and/or a "carriage return" must separate the fuse number from the fuse states. The stream of fuse states can be as long as desired (up to the maximum allowable fuse number). The fuse data for an entire device, for example, could be sent in one "L" field starting at zero and continuing for all fuses in the device. Spaces and carriage returns may be inserted to make the stream more readable. Each "L" field must be terminated with an asterisk.

The "C" field is the sum-check of the entire fuse RAM (fuse number 0 to maximum fuse number for the selected device), not just the fuse states sent. See figure 3-13. (The JEDEC term "Fuse Checksum" is the same as Data I/O's term "sum-check.")

```
⟨STX⟩*⟨ETX⟩002F          02 + 2A + 03 = 2F


random text ⟨return⟩⟨line feed⟩                                    = 0000
⟨STX⟩TEST*⟨return⟩⟨line feed⟩        02+54+45+53+54+2A+0D+0A = 0183
QF0384*⟨return⟩⟨line feed⟩        51+46+30+33+38+34+2A+0D+0A = 01A7
F0*  ⟨return⟩⟨line feed⟩                46+30+2A+20+20+0D+0A = 00F7
L10 101*⟨return⟩⟨line feed⟩  4C+31+30+20+31+30+31+2A+0D+0A = 01A0
⟨ETX⟩05C4 ⟨return⟩ other random text                      03 = 0003
                                                                 ----
                                                                 05C4
```

Figure 3-12. Computing the Transmission Checksum

The structured test vector information is specified by the "QP", "P", and "V" fields. The "QP" field defines the number of pins on the device. The "V" field starts with a vector number, is followed by a space, then by a series of test conditions for each pin, then is terminated with an asterisk. The test conditions are normally sent in pin number order; however, the "P" field can specify a different sequence. The PLDS JEDEC translator does not validate the test conditions in the vectors (see table 3-3 for the presently defined test conditions). The supervoltage test conditions (2 through 9) are used to apply non-TTL levels to certain pins to access special test features. A device could be damaged by improper use of supervoltages.

The Logic Fingerprint™ test information is specified by the "T", "S", and "R" fields. The "T" field defines the number of test cycles to be performed. The legal values are Ø to 99 decimal. The "S" field defines the starting vector with a series of 1s and Øs for each pin. The "R" field defines the 8-digit hexadecimal Logic Fingerprint™ test signature.

The "G" field defines the security fuse state.

The "D" field is not sent by new versions of the PLDS JEDEC translator. It has been replaced by the "QF" and "QP" fields and the manual setting of family codes and pinout codes.

Transmit JEDEC Data

This command transmits the contents of the fuse and vector RAM to the serial port in the JEDEC format (see appendix A of the LogicPak™ manual).

The following characteristics apply to JEDEC transmission:

- The output may be halted by sending a *CONTROL S* (*DC1* ASCII, *11* hex) and restarted by sending a *CONTROL Q* (*DC3* or ASCII, *13* hex).
- An *ESC* character (ASCII, *1B* hex) will abort the transmission and return to the programmer front panel operation.
- A *CONTROL Y* (ASCII, *19* hex) will terminate the transmission and return to the terminal or programmer front panel operation.
- The Logic Fingerprint™ test fields (S, R, and T) are not sent if the number of cycles is Ø.
- The "G" field is sent only if security fuse data is a "1."
- The fuse checksum (C field) is the 16-bit sum of all fuse states (i.e., from fuse Ø to the fuse limit for the device). See figure 3-13.

```
(STX)*F0*L0000
01001110 00001000 11110000 11111111 01010001*
C021A*
(ETX)0000

The F0* cleared all the fuse RAM to 0. The L field transmitted 40
fuse states starting at 0.

Fuse number  00 01 02 03 04 05 06 07  08 09 10 11 12 13 14 15  16
State         0  1  0  0  1  1  1  0   0  0  0  0  1  0  0  0   1


                MSB              LSB

                 7 6 5 4 3 2 1 0

  0000           0 1 1 1 0 0 1 0          72
  0008           0 0 0 1 0 0 0 0          10
  0016           0 0 0 0 1 1 1 1          0F
  0024           1 1 1 1 1 1 1 1          FF
  0032           1 0 0 0 1 0 1 0          8A
  0040           0 0 0 0 0 0 0 0          00
  0048           0 0 0 0 0 0 0 0          00
  xxxx           0 0 0 0 0 0 0 0          00
                                         ----
                                         021A
```

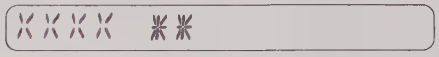
Figure 3-13. Computing the Fuse RAM Checksum

Front Panel Control

To transmit JEDEC data, follow the steps below.

Model 29 Displays

Model 29 Displays



NOTE

□ is the action symbol. XXXX is the fuse array sum-check.

Terminal Control

To transmit JEDEC data from the terminal mode, enter a "C" from the Command mode:

See figure 3-10 for the terminal display of the Basic Gates design example data.

Receive JEDEC Data

This command prepares the programmer to receive fuse and vector data from a peripheral device via the serial port. A translator converts the JEDEC format data (see appendix A of the LogicPak™ manual) to the memory image required by the PLDS.

NOTE

The D field is ignored by the translator. The correct family code and pinout code must be entered before receiving JEDEC data. See table A-1 in appendix A for correct family codes and pinout codes.

Three types of errors may be caused by receiving improper data in the JEDEC format (see table 3-6).

Table 3-6. Translator Input Errors

ERROR	DESCRIPTION	POSSIBLE FIELDS
82	SUMCHK ERR	Transmission check-sum
84	INVALID DATA	ETX F L S V
91	I/O FORM ERR	C G L P R T V

You may determine the field in which the error occurred by examining data RAM location 0408; the ASCII value (hexadecimal) of the field is stored here (see table 3-7). More information about the possible cause of the error may be found in table 3-8.

Table 3-7. ASCII Values of Field Identifiers

FIELD IDENTIFIER	ASCII CHARACTER HEX VALUE
(ETX)	03
C	43
F	46
G	47
L	4C
P	50
R	52
S	53
T	54
V	56

To examine the data RAM location 0408, perform these steps.

Model 29 Displays

Model 29 Displays

NOTE

XXXX is the current address. XX is the field identifier in hexadecimal.

The transmission checksum computed by the PLDS may be found by examining data RAM locations 405 and 406 in a similar manner.

Front Panel Control

To receive JEDEC data from the front panel mode perform the steps which follow.

Model 29 Displays

Model 29 Displays

NOTE

□ is the action symbol. XXXX is the fuse array sum-check.

Table 3-8. Translator Input Error Codes

ERROR	DISPLAY	FIELD*	POSSIBLE CAUSE
82	SUMCHK ERR	ETX	Transmission checksum of all ASCII characters does not match the computed value.
84	INVALID DATA	ETX	Fuse sum-check does not match computed sum-check. The comparison is not made until the transmission is complete, so the field is stored as ETX rather than C. The sum-check includes the entire fuse RAM as defined by the family and pinout code, not just the fuse states sent.
		F	Invalid character in field. Only "1" and "0" are allowed.
		L	A space or carriage return did not follow the fuse number.
		L	An invalid character was in the fuse state field. Only "1" and "0" are allowed. Spaces, line feeds, and carriage returns are ignored.
		S	Invalid character in field. Only "1", "0", and "N" are allowed.
		V	Too few or too many test conditions.
91	I/O FORM ERROR	C	Invalid character in field, must be 4-digit hexadecimal number.
		G	Invalid character in field. Only "1" or "0" are allowed.
		L	Fuse number exceeds fuse limit for device or invalid fuse number (must be decimal number).
		P	Too few or too many pins or invalid pin number for device.
		T	Test cycles greater than 99.
		R	Invalid character in field: must be 8-digit hexadecimal number.

*From RAM Addr. 0408

Terminal Control

To receive JEDEC data from the terminal mode, enter a "B" from the Command mode:

Terminal Displays

3.5.10 EDIT FUSE PATTERN

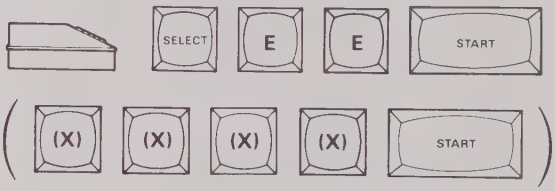
The individual fuses that make up a PAL® Fuse map may be edited using the fuse map editor. Fuses may be changed from blown to unblown or vice-versa on a downloaded fuse map, a fuse map generated by assembly of source code, or directly in fuse memory.

Fuses may be edited one at a time from the front panel, or in line editor fashion from a terminal. In the examples that follow, assume that we are editing the Basic Gates fuse map of figure 3-8, representing the logic diagram of figure 3-9.

If "Device Selection Error" appears when you enter the fuse editor, you must specify the family code and pinout code to define the fuse map.

Front Panel Control

Enter the fuse editor with select code *EE:*



Model 29 Displays

XXXX is decimal number of fuse being edited; ** is binary state of fuse number *XXXX (00 or 01).*

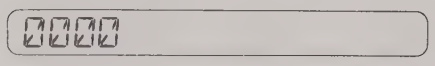
The desired fuse number for editing from the front panel may be scrolled to by using the *START* and *REVIEW* keys, or specified directly by entering the fuse number *XXXX,* as shown above. The data displayed on the right reflects the current state of the selected fuse:

01 = high-resistance, "blown" fuse
00 = low-resistance, fuse intact

Entering a 0 or a 1 while displaying a selected fuse will store that state for the fuse.

To change fuse number 98 in our Basic Gates example from unblown to blown:

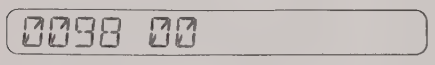
Model 29 Displays



Fuse number

Enter the decimal fuse number, 98.

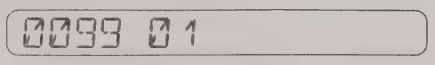
Model 29 Displays



Fuse state

This display indicates that RAM data for fuse 98 is set for "don't program." To change it to a programmed (blown) state:

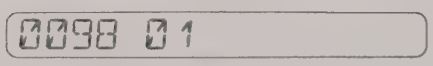
Model 29 Displays



(Fuse number increments automatically.)

To decrement a fuse number:

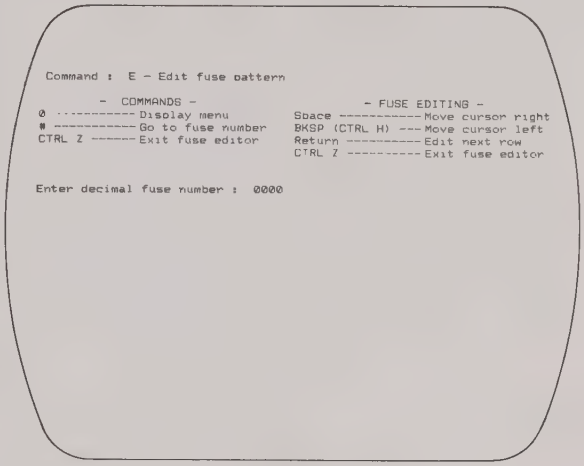
Model 29 Displays



Terminal Control

Enter an *E* from the terminal Command mode:

Terminal Displays


Command : E - Edit fuse pattern
- COMMANDS -
Ø ---------- Display menu
---------- Go to fuse number
CTRL Z ------ Exit fuse editor
- FUSE EDITING -
Space ---------- Move cursor right
BKSP (CTRL H) --- Move cursor left
Return ---------- Edit next row
CTRL Z ---------- Exit fuse editor
Enter decimal fuse number : 0000

You may now specify a fuse number directly, or enter *RETURN* to display the first fuse row.

The fuse editor is a fixed-format line editor, with the first column of the displayed line reserved for command characters. A character entered in the first column (normally blank) is interpreted as a command and acted upon immediately; otherwise, fuse editing is not processed until a *RETURN* is entered (at any point on the line). The command characters recognized in the first column are Ø (zero) and #.

The fuse editor display (see figure 3-14) shows the specified fuse number followed by the next *N* consecutive fuses, where *N* is the number of fuses in one row of the selected PAL. Any fuse number may be specified, regardless of row boundaries, and the display will follow this convention. Thus, entering *RETURN* at any time moves the editor to the fuse one row down from the previously specified fuse. Index marks are shown over every tenth fuse in the row displayed, for easy location of fuses beyond the one specified. Also, note that the fuse display may be changed from X/- to 0/1 with select code *CE* or main menu command G (see subsection 3.5.12).

In operation, the fuse editor copies the selected row to a temporary buffer where all editing changes are made. Then, when a command or *RETURN* is entered, the editing buffer is examined for legal characters before copying back to the fuse map. You are not allowed to proceed to another row until all characters are legal in the current row. Typing a *CTRL Z* to exit the fuse editor from an untested edited row will leave the row in its original state.

To edit a fuse row, use the following procedure:

1. Move the cursor back and forth along the displayed row using *SPACE* and *BACKSPACE* until it is positioned over the fuse to be changed.
2. Press the desired symbol to enter it into the editing buffer as the fuse state.
3. Enter Ø (zero) or # in the command character position at any time to display the menu or move to a specific fuse number.
4. Press *RETURN* at any time to move to the next row.
5. Press *CTRL Z* at any time to exit the fuse editor.

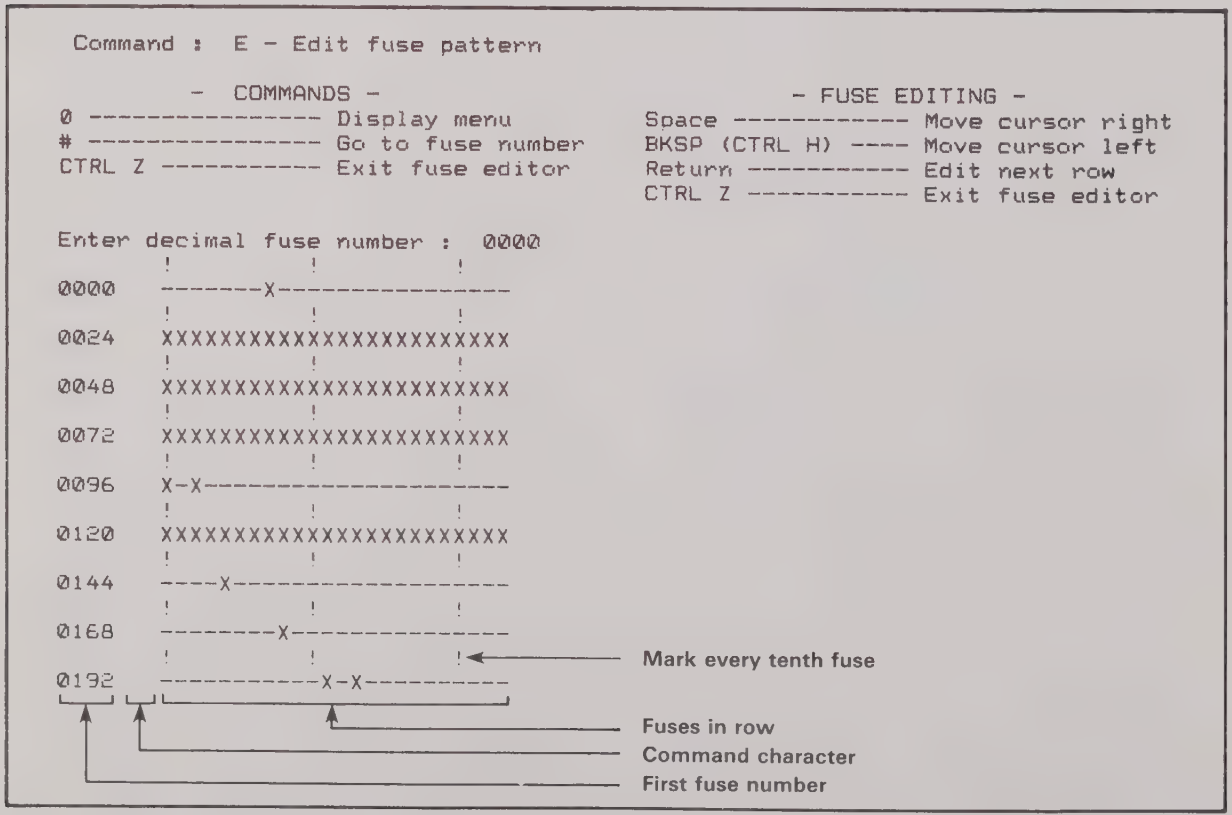


Figure 3-14. Default Fuse Editor Pattern

Editing fuse number 98 in our example may be done in two ways. As one method, you can enter the fuse editor and type *RETURN* until the desired row appears (beginning with fuse 0096), resulting in a display that matches the device data sheet, and then space three times to locate fuse 98. The display in this case will resemble figure 3-14.

Alternatively, fuse number 98 may be directly specified. When this is done, a fuse "row" is displayed which begins with fuse number 0098 and does not match any of the rows in the logic diagram of figure 3-9. Fuse number 98 may now be modified without counting spaces, and subsequent *RETURN*s will jump to the fuses directly below fuse 98 in the same column (122, 146, 170, etc.). Figure 3-16 shows the display when this method is used.

```
Enter decimal fuse number :  0098
          '         '         '
0098   X----------------------XX
          '         '         '
0122   XXXXXXXXXXXXXXXXXXXXX--
          '         '         '
0146   --X--------------------
          '         '
0170   ------X----------------
```

Figure 3-15. Starting Fuse Not on Row Boundary

3.5.11 DISPLAY CONFIGURATION NUMBER

This command displays the configuration number of the adapter firmware. Configuration numbers are used as serial numbers for firmware.

Front Panel Control

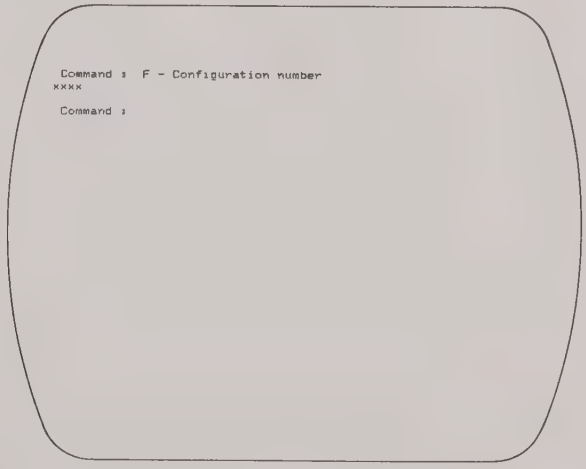
Enter SELECT *EF* from the front panel:

Model 29 Displays

Terminal Control

Enter an *F* from the terminal command mode:

Terminal Displays



NOTE

XXXX *is the configuration number of the firmware in the adapter plugged into the PLDS.*

3.5.12 SELECT ATTRIBUTES

This command allows you to select one of two options for any of six attributes, as shown below. The only options available to the PALASM and H & L design adapters are those numbered Ø thru 7:

OPTION	DESCRIPTION
Ø	Echo (full duplex): PLDS echoes all characters received at the serial port.
1	No echo (half duplex).

NOTE

The default echo mode will depend upon the programmer being used. The Model 29 and 100A programmers will power up in the "no echo" mode, while the Model 19 will power up in the echo mode.

2	JEDEC full mode: described by the JEDEC standard (JC-42-1-81-62). This is the default state.
3	JEDEC kernel mode: selects the kernel mode (see appendix A of the LogicPak™ manual for kernel mode definition).
4	Fuse display X/—: displays an unprogrammed fuse as "X" and a programmed fuse as a "-". This is the default state.
5	Fuse display 0/1: displays an unprogrammed fuse as "0" and a programmed fuse as "1".
6	End upload with *ETX*: PLDS terminates an upload operation (serial data transmission) with an *ETX* character (ASCII hex *Ø3*). *This is the default state.*
7	*End upload with CTRL Z*: ends the upload with a *CTRL Z*.

An underblow condition occurs when the programmer RAM indicates that a particular fuse should be blown and the device in the socket shows the fuse to be unblown. An overblow condition occurs when the programmer RAM indicates that a fuse is unblown, yet the part shows it to be blown.

8	Disable underblow/overblow display: disables this attribute.
9	Enable underblow/overblow display: enables this attribute.
A	Two-pass functional verify: performs the normal two-pass functional verify at V_{CC} voltages above and below nominal.
B	One-pass functional verify: speeds up the testing cycle by doing only a one-pass functional verify at the nominal V_{CC} voltage.

Front Panel Control

To access the attributes from the front panel, do the following:

Model 29 Displays

To change any attribute, enter the code number from those given above, where the (*X*) is shown in the following key sequence.

Model 29 Displays

Terminal Control

To access the attributes from the terminal, enter a *G* from the command mode.

Terminal Displays

```
Command : G - Select attributes

0 - Echo (full duplex)
1 - No echo (half duplex)

2 - JEDEC full mode (default)
3 - JEDEC kernel mode

4 - Fuse display X/- (default)
5 - Fuse display 0/1

6 - End upload with ETX (default)
7 - End upload with CTRL Z

8 - Disable underblow/overblow display (default)
9 - Enable underblow/overblow display

A - Two pass functional verify (default)
B - One pass functional verify

Options: 0,2,4,6,8,A
```

To change an attribute or attributes from the terminal, space or backspace (*CTRL H*) to the appropriate attribute(s) and enter the new value. The edit session is terminated by a *RETURN* if the edited attribute(s) are to be saved or by a *CTRL Z* if they are not to be saved. If an invalid value is entered, the line will be repeated, including the invalid data, waiting for the correct value(s) to be entered.

3.5.13 EXIT COMMANDS

During terminal mode, a *CTRL Z* will exit specific operating modes. When using the design adapters, this function is also used to terminate the change, insert, and edit modes.

simultaneously

Terminal Displays

```
Command :
```

The *ESC* (escape) key is used to terminate all PLDS operations and return control to the front panel. This must be done before removing an adapter or the LogicPak™.

returns control to the programmer front panel from terminal control.

3.6 MMI REGISTERED PAL® PRESET INFORMATION

The 303A-002 P/T adapter contains an auto-preset feature for registered PAL®s with pinout code less than 30. Since the device registers do not power-on to a known state, this auto-preset feature sets the registers to a known state so that the Logic Fingerprint™ test can be performed without first having to intentionally preset the registers, as outlined in section 1.3 under Fingerprint Limitation 3. This feature is enabled whenever functional testing is performed on MMI Registered PAL®s.

There is, however, one limitation of this preset feature: When the security fuse has been blown in the device, the registers will preset to a different state. This will cause a different Logic Fingerprint™ test-sum to be calculated for a good device, one with the security fuse blown, to generate this second Logic Fingerprint™ test-sum for newly programmed parts to be checked against. This second Logic Fingerprint™ test-sum can then be recorded for future manual entry or stored in a JEDEC format file.

SECTION 4
CALIBRATION AND TROUBLESHOOTING

4.1 OVERVIEW

WARNING

The instructions in this section are for qualified service personnel only. Do not attempt to perform them unless you are qualified.

The material in this section is provided to help you keep your LogicPak™ and P/T adapter in optimum operating condition. For users who prefer to do their own calibration, detailed procedures, including measurement charts and timing diagrams for each device, are provided. The basic procedures to set up the LogicPak™ in the calibration mode are described in subsection 4.2.

4.2 CALIBRATION

The need for calibration varies with the amount of use your LogicPak™ receives. Generally, we suggest calibration whenever: (1) programming yields fall below the manufacturer's recommended minimums, (2) when troubleshooting has been completed, or (3) if your company policy requires periodic calibration certification. Because the LogicPak™ must be calibrated with an adapter installed and the values vary with different adapters, the detailed calibration procedures, measurement charts, and timing diagrams are provided in this manual. The calibration setup procedure is described in this section.

NOTE

If calibration or repair is required, but you lack the facilities to accomplish it, contact the nearest Data I/O Service Center. Because of the different programmer mainframes and adapters, this manual does not attempt to cover all areas of programmer calibration. Instead, it lists the steps necessary to calibrate only the LogicPak™ and adapter.

To prepare the LogicPak™ for calibration:

1. Remove the adapter (if any) from the LogicPak™ (see subsection 2.3).
2. Remove the four Phillips-head screws on the top of the LogicPak™ cover (see figure 4-1).
3. Remove the two Allen screws on each side of the LogicPak™ cover (see figure 4-1).
4. Lift the cover off the circuit board cage assembly.
5. Plug the adapter into the connector on the pin driver board as shown in figure 4-2.
6. Plug the LogicPak™ into the programmer.

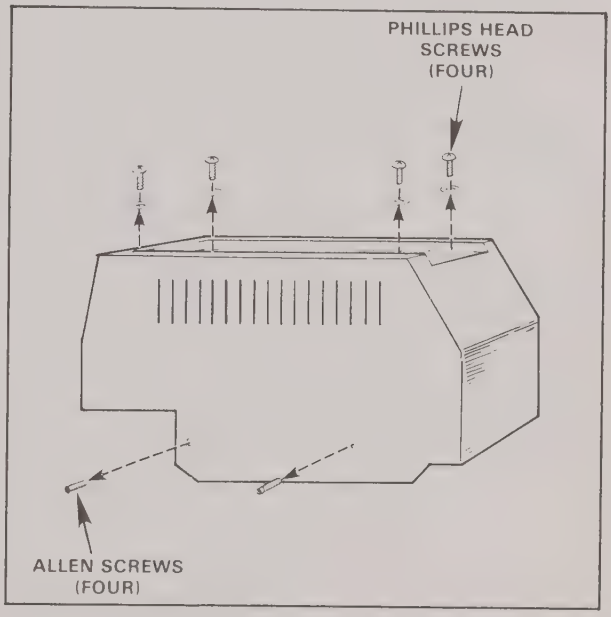


Figure 4-1. LogicPak™ Cover Removal

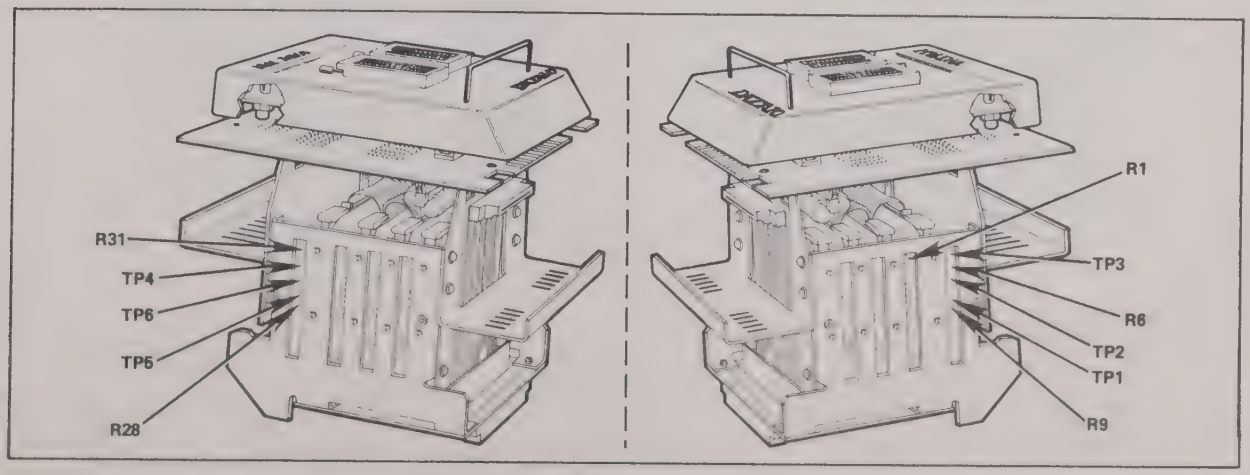


Figure 4-2. Calibration Equipment Setup

Calibration of the LogicPak™ and adapter consists of three parts:

1. Power supply calibration--measures the DC supply voltages of the programmer. All other voltages depend on these supplies; therefore, this part of the calibration procedure must be done first. Refer to your programmer manual.
2. DC calibration--consists of measuring and adjusting critical DC voltage levels generated by the LogicPak™ and by the adapter.
3. Waveform observation--enables observation of waveforms on an oscilloscope to ensure compliance with the device manufacturers' critical voltage and timing specifications.

Because the first part of the calibration procedure (power supply calibration) varies with the type of programmer you have, this manual refers you to your programmer manual for details on power supply calibration. DC calibration is discussed in subsection 4.2.1 and waveform observation is detailed in subsection 4.2.2. For information on how to carry out these steps on various programmers, consult your programmer manual.

The following equipment is necessary to calibrate the LogicPak™:

- 3½-digit digital voltmeter (DVM)
- Dual-trace oscilloscope (Tektronix 465 or equivalent)

4.2.1 DC CALIBRATION (Steps 1-10 and 12)

These DC calibration procedures enable you to adjust critical DC voltage levels generated by the LogicPak™ and adapter. To follow these procedures, use the measurement chart at the back of this section (table 4-3), which contains the information necessary for all DC calibration tests. This information is included on the measurement chart in columns with the following headings:

- Step No.--tells which step to use for each test. Step numbers are set at the programmer keyboard and reflected in the display.
- Test No.--identifies individual tests.
- Test description--identifies the functions being tested.
- Measurement location--tells which socket pins or circuit board test points to probe for measuring voltages.
- Measurement--specifies allowable measurement ranges. If a reading falls outside the range and you cannot adjust it to within the range, do not use the LogicPak™ until the problem is corrected.
- Adjustment location--tells which potentiometer to adjust if a measurement is out of range.
- Comments--gives special instructions for particular tests.

The DC calibration procedures follow.

CAUTION

Remove all devices from the sockets before entering the calibration mode (see subsection 3.4.3 for details). Calibration voltages may damage any device in the LogicPak™ sockets.

1. Turn the programmer power on.

NOTE

If left in calibration steps 1 through 7 for more than 5 minutes without a front panel key depression, the machine will reset itself.

2. Put the programmer into the calibration mode by following the key sequences in table 4-1. The table also explains how to increment or decrement the step number and how to enter calibration at an advanced step (which is required during the waveform calibration part of the process).
3. Perform the general calibration steps (steps 1-10 and 16) on the measurement chart.

Table 4-1. Key Sequence To Access the Calibration Mode

Programmer System	Key Sequence To Enter Calibration Mode	To Increment Step No.	To Decrement Step No.
19	Press *SELECT* Press *C2* Press *ENTER* Enter Step Number[a] Press *START*	Press *ENTER*	Press *REVIEW*
Model 29	Press *SELECT* Press *C1* Press *START* *Enter Step Number*[a] *Press START*	Press *START*	Press *REVIEW*
100A	Press *SELECT* Press *12* Enter Step Number[a] Press *START*	Press *START*	Press *BACKSPACE*

[a]Optional

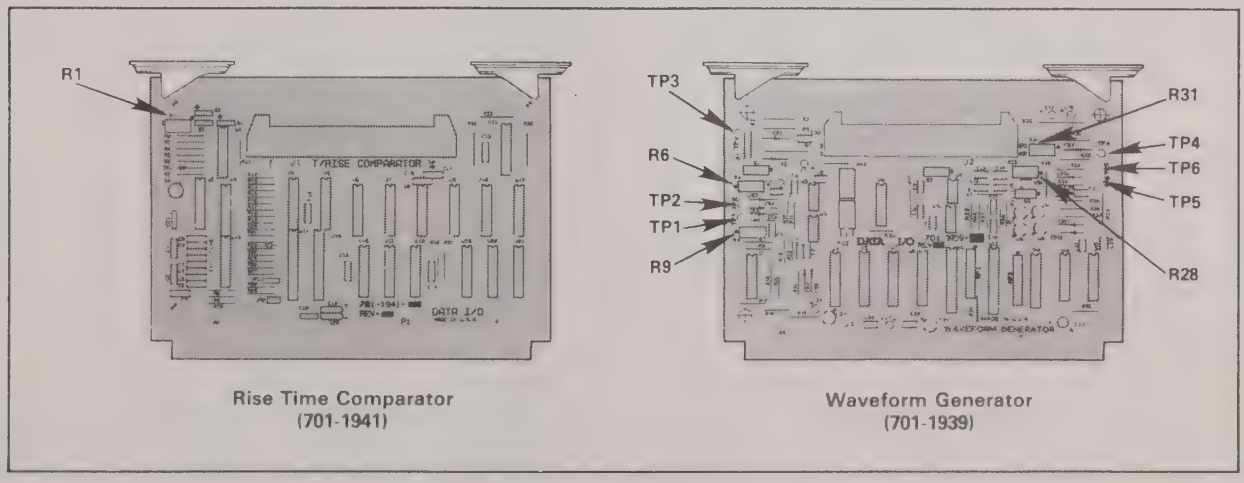
CAUTION

If the LogicPak™ fails the second step on the measurement chart, do not proceed to the next step. The hardware must pass this step or further testing may damage the LogicPak™.

If the LogicPak™ fails any step on the measurement chart, do not continue to the next step. Refer to table 4-2, which lists error codes and descriptions. Subsequent tests will not give valid results unless all preceding steps are passed and adjustments made.

For each general calibration step on the measurement chart:

- Take measurement readings at the device sockets or test points indicated in the measurement chart.
- Ground the DVM to pin 10 on a 20-pin socket, to pin 12 on a 24-pin socket, or to pin 14 on a 28-pin socket.
- The oscilloscope trigger point is called out on the measurement chart photographs.
- The adjustment potentiometers on the waveform generator and the T/rise comparator card enable you to make adjustments when your measurements do not match the measurement chart; figure 4-3 shows the location of these adjustment points.
- Access each new step by pressing *START* (or *ENTER*). The new step number will appear on the display when the LogicPak™ is ready for the next step. To return to a previous test, press the *REVIEW* (or *BACKSPACE*) key.



Rise Time Comparator (701-1941)

Waveform Generator (701-1939)

Figure 4-3. LogicPak™ Test and Adjustment Locations

Table 4-2. PLDS Error Codes

ERROR CODE	DESCRIPTION	ACTION
21*	Illegal-Bit Error	The programmer is asked to leave intact a fuse which is already blown. Examine programmer RAM and the device's data.
22*	Programming Error	An attempt to blow a fuse was made and failed. Try the programming sequence again. If the second attempt also fails, try another device. If both devices produce this error, check the calibration of the LogicPak™. If calibrated correctly, contact your local Data I/O office.
25*	No Socket Adapter	Insert appropriate socket adapter.
30	No (or Invalid) Device Selected	Enter valid device family and pinout codes (refer to table A-1).
31*	Overcurrent	Hardware error in LogicPak™ or shorted device. Substitute a known-good device or consult the troubleshooting section of the LogicPak™.
32*	Backward Device/V_{CC} Overcurrent	(1) Device plugged in backward; turn it around. (2) V_{CC} overcurrent, probably caused by a faulty device.
33	Extended RAM Fail (Occurs only when PALASM adapter is installed.)	PALASM source file exceeds source buffer size.
34	Invalid Device Selected	Incorrect family and pinout codes entered. Enter proper family pinout code. This error occurs in computer remote control only.
35	Source Equation Translation Error	Check equation buffer by connecting terminal to examine the equation buffer. This error code lets the operator know that an error exists in the source equations when the programmer is not controlled by a terminal.
36	Begin RAM Pointer Not = 0000	Refer to programmer manual to reset the begin RAM pointer to zero. This error usually occurs when changing from one programming pak to another.
37	Invalid Device-Related Operation	Verify, program, or other illegal operation was attempted, with a design adapter installed.
38*	Calibration Step Error	(1) Indicates you have selected an incorrect calibration step, or (2) a program operation is attempted prior to exiting calibration—exit the calibration mode (refer to the programmer manual).
63	RAM Write Error	System RAM failure. Refer to programmer manual or contact Data I/O service representative.
65	Firmware Sum-Check Error	This indicates that the EPROM firmware in the LogicPak™ or adapter may have changed since the unit was shipped. Contact Data I/O service representative. Do not continue operation until the situation is corrected.
70*	DAC Error, V_{CC}	See subsection 4.4 (troubleshooting) of LogicPak™ manual.

*These errors do not apply to design adapters.

(Continued)

Table 4-2. PLDS Error Codes (Continued)

ERROR CODE	DESCRIPTION	ACTION
71*	DAC Error, Bit Switch Number 1	See subsection 4.4 of LogicPak™ manual.
72*	DAC Error, Bit Switch Number 2	See subsection 4.4 of LogicPak™ manual.
73*	DAC Error, CE	See subsection 4.4 of LogicPak™ manual.
74*	Logic Fingerprint™ Test Verify Error	Indicates one of the following Logic Fingerprint™ errors: (1) Device passed fuse verify but failed Logic Fingerprint™ test—defective device. (2) Operator has entered wrong test-sum. (3) Device cannot be tested with Logic Fingerprint™ (refer to subsection 1.3 for the limitations of the Logic Fingerprint™ test).
75	Structured Test Verify Error	The device passed fuse verify but failed structured test—defective device. Check structured test vectors and make sure they are correct. If not, enter the correct vectors. The vector could be invalid, or the operator may have miskeyed a valid vector.
76	Self-Test Error	This indicates failure in the LogicPak™. Consult subsection 4.4 (troubleshooting) of LogicPak™ manual or contact your Data I/O service representative.
77	Security Fuse Programming Error	(1) Indicates that the security fuse option cannot be programmed in the installed device, or (2) there is no security fuse option available for this type of device.
78*	No Fuse Verify Set	Indicates you have tried to program the device with the verify-option mode set for 2. The verify option will not allow this. When this error code displays, select E6 and enter Ø or 1, and then you will be allowed to program the device.
79*	Preload Not Implemented	The preload algorithm is not implemented for this device.
81	Parity Error	A parity error occurred while receiving serial data.
82	Checksum Error	Indicates an incorrect transmission of data from a peripheral to the serial port, including fuse data, CRs, STX, etc.
84	Invalid Data	See subsection 3.5.9 of LogicPak™ manual.
91	Fuse Address Error	See subsection 3.5.9 of LogicPak™ manual.

*These errors do not apply to design adapters.

[a]See LogicPak™ manual for locations of I/O pins.

4.2.2 WAVEFORM OBSERVATION

Programming waveforms of your LogicPak™ can be observed with an oscilloscope and compared with the timing diagrams at the end of this section. In this way, timing and magnitude relationships can be measured against known specifications to confirm that the LogicPak™ is performing to the device manufacturer's specifications. Step 13 displays the verification waveforms, and step 14 displays the programming waveforms for selected family and pinout codes and fuse numbers. When step 15 is called, the waveforms will reflect the programming algorithm for only the fuses to be programmed as specified in RAM. To alter the state of the individual fuses, refer to subsection 3.5.10, Edit Fuse Pattern. Because the LogicPak™ generates many waveforms, and all calibration adjustments are accomplished in DC calibration, it is necessary only to observe waveforms for commonly used devices or devices that are presenting yield problems. These measurements can be performed on any device by entering the appropriate family and pinout codes and fuse number (if appropriate).

4.2.3 EXPLANATION OF TIMING DIAGRAMS

This manual contains a set of timing diagrams for the MMI/National family of logic devices. The timing diagrams show critical waveforms for a specific device but may be verified for any of the MMI/National devices by entering the appropriate family and pinout code before invoking the calibration mode. To use these diagrams and photographs, read the information provided below and refer to the sample timing diagram (figure 4-4).

1. Family and Pinout Code Number--corresponds to the family and pinout code numbers of the device.
2. Waveform Variables--lists the minimum and maximum parameter values; voltage and timing parameters other than those listed in this table are to be considered noncritical with a ±10% tolerance.
3. Notes--important information pertaining to a timing diagram.
4. Waveform Names--the manufacturer's reference to the pin being observed.
5. Layout Sequence Number--used as a reference point within each diagram.
6. Delay Time Position--indicates the time from the start of the main sweep to the start of the delay time.
7. Oscilloscope Ground Reference--ground pin (pin 10) of the socket.
8. Time-Base Setting--Horizontal positioning of the waveforms is not critical and may vary slightly from the photographs. The important observation is the timing relationship between the waveforms in the photographs. You can adjust this timing relationship on your oscilloscope to set convenient reference points. By considering any time-base variance, you can also make time comparisons between photographs. The time base is always the same for different waveforms in the same photograph.
9. Voltage--indicates volts per division. The one in the upper-left corner is for the top trace and the one in the lower-left corner is for the bottom trace.
10. Pin Name and Number--the device pin name and socket pin number where the waveform can be observed.

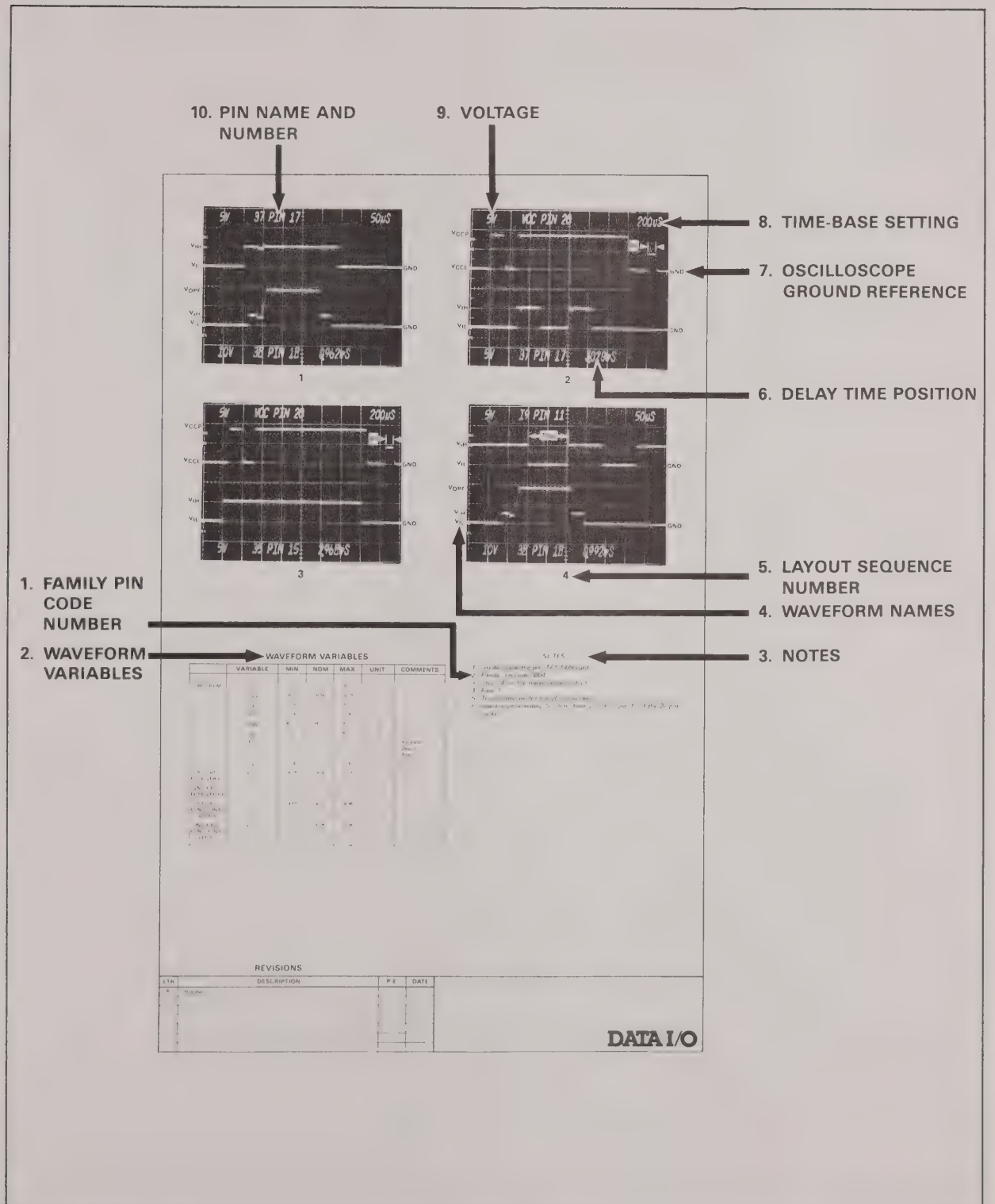


Figure 4-4. Sample Timing Diagram

Measurement Charts

REVISIONS

LTR	DESCRIPTION	P.E.	DATE
A	Release	KM	4/26/65

Table 4-3. Measurement Chart for MMI National PAL® Adapter

10-715-1965 (303A-002)

STEP	TEST NO.	TEST DESCRIPTION	MEASUREMENT LOCATION Socket/pins or circuit board test points	MEASUREMENT MIN	MEASUREMENT NOM	MEASUREMENT MAX	ADJUSTMENT LOCATION	COMMENTS Ground pin 10 or 12[a]
1	1	All pins low	24 pin/all pins	-0.4		0.8		CAUTION[b]
			20 pin/all pins					
2	2	Self-test, sink drivers						See table 4-4 if errors result;
								errors must be corrected to
								continue. Possible errors are
								A0-DF.
3	3	LED test 1						Confirm 24-pin LED on, 20-pin off
								For test 5-19, see note[c].
	4	Comparator reference	701-1939/TP5	10.20	10.24	10.28	R28/701-1939	
								CAUTION[d]
	5	V_{CC} supply	24 pin/pin 24	11. 9	12.0	12.1	R9/701-1939	Load with 50Ω 5W resistor to
			20 pin/pin 20					ground.[d]
	6	CE supply	24 pin/pin 13	19.8	20.0	20.2	R31/701-1939	Load with 100Ω 5W resistor to
								ground.[d]
	7	Bit supply SW 1	24 pin/pin 19	19.8	20.0	20.2	R6/701-1939	Load with 100Ω 5W resistor to
								ground.[d]
	8	Bit supply SW 2	24 pin/pin 14	19.6		20.4		Load with 100Ω 5W resistor to
								ground.[d]
	9	DAC reference	701-1939/TP6	4.7		5.3		

CAUTION: DO NOT POWER DOWN AFTER STEP 1.

[a] Connect the ground of the DVM to ground pin 10 on a 20-pin socket, to pin 12 on a 24-pin socket, or to pin 14 on a 28-pin socket.
[b] Do not leave programmer unattended in calibration mode beyond step 1.
[c] Voltage levels are for calibration purposes only and are not the specified levels of the device manufacturer. For manufacturer-specific levels refer to step 12.
[d] Insert load resistor after pressing START; remove immediately after performing test.

SECTION 4
CALIBRATION AND TROUBLESHOOTING

4.1 OVERVIEW

The material in this section is provided to help you keep your LogicPak™ and P/T adapter in optimum operating condition. For users who prefer to do their own calibration, detailed procedures, including measurement charts and timing diagrams (section 4.2) for each device, are provided. The basic procedures to set up the LogicPak™ in the calibration mode are described in section 4.2.

4.2 CALIBRATION

The need for calibration varies with the amount of use your LogicPak™ receives. Generally, we suggest calibration whenever: 1) programming yields fall below the manufacturer's recommended minimums, 2) when troubleshooting has been completed, or 3) if your company policy requires periodic calibration certification. Because the LogicPak™ must be calibrated with an adapter installed and the values vary with different adapters, the detailed calibration procedures, measurement charts, and timing diagrams are provided in each adapter manual. The calibration setup procedure is described in this section.

NOTE

If calibration or repair is required, but you lack the facilities to accomplish it, contact the nearest Data I/O Service Center. Because of the different programmer mainframes and adapters this manual does not attempt to cover all areas of programmer calibration. Instead, it lists the steps necessary to calibrate only the LogicPak™.

To prepare the LogicPak™ for calibration:

1. Remove the adapter (if any) from the LogicPak™ (see section 2.3).
2. Remove the four phillips-head screws on the top of the LogicPak™ cover (see figure 4-1).
3. Remove the two allen screws on each side of the LogicPak™ cover (see figure 4-1).
4. Lift the cover off the circuit board cage assembly.
5. Plug the adapter into the connector on the pin driver board as shown in figure 4-2.
6. Plug the LogicPak™ into the programmer.

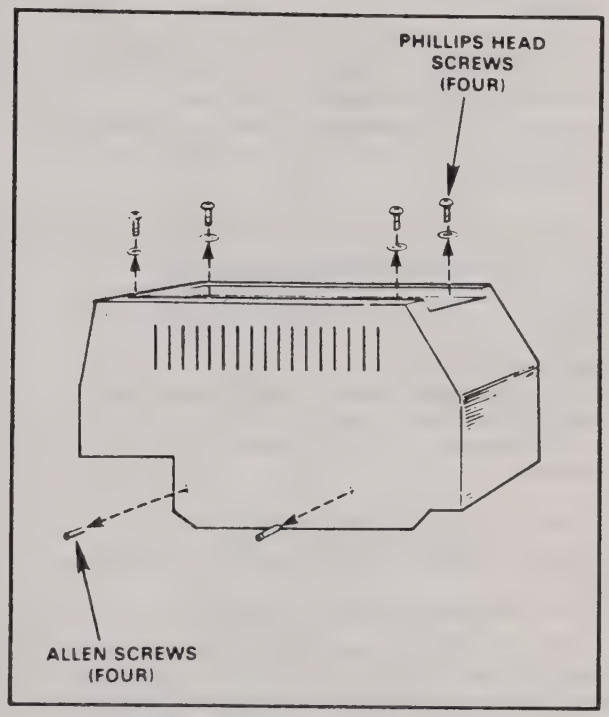


Figure 4-1. LogicPak™ Cover Removal

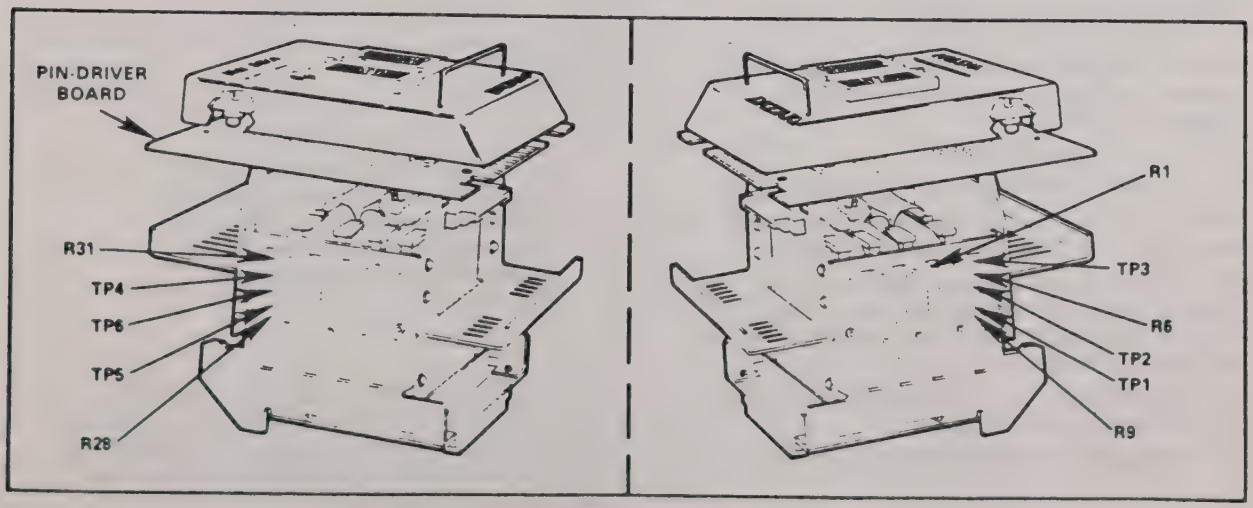


Figure 4-2. Calibration Equipment Setup

Because of the different programmer mainframes, this manual does not cover all areas of programmer calibration. Instead, it lists the steps necessary to calibrate only the LogicPak™ and adapter.

Calibration of the LogicPak™ and adapter consists of three parts:

1. Power supply calibration--measures the DC supply voltages of the programmer. All other voltages depend on these supplies; therefore, this part of the calibration procedure must be done first. Refer to your programmer manual.
2. DC calibration--consists of measuring and adjusting critical DC voltage levels generated by the LogicPak™.
3. Waveform observation--enables observation of waveforms on an oscilloscope to ensure compliance with the device manufacturers' critical voltage and timing specifications.

Because the first part of the calibration procedure (power supply calibration) varies with the type of programmer you have, this manual refers you to your programmer manual for details on power supply calibration. DC calibration is discussed in section 4.2.1 and waveform observation is detailed in section 4.2.2. For information on how to carry out these steps on various programmers, consult your programmer manual.

The following equipment is necessary to calibrate the LogicPak™:

- Three-and-a-half-digit digital voltmeter (DVM)
- Dual-trace oscilloscope (Tektronix 465 or equivalent)

4.2.1 DC CALIBRATION (Steps 1-10 and 12)

These DC calibration procedures enable you to adjust critical DC voltage levels generated by the LogicPak™. To follow these procedures use the measurement chart at the back of this section (table 4-3), which contains the information necessary for all DC calibration tests. This information is included on the measurement chart in columns with the following headings:

- Step No.--tells which step to use for each test. Step numbers are set at the programmer keyboard and reflected in the display.
- Test No.--identifies individual tests.
- Test description--identifies the functions being tested.
- Measurement location--tells which socket pins or circuit board test points to probe for measuring voltages.
- Measurement--specifies allowable measurement ranges. If a reading falls outside the range and you cannot adjust it to within the range, do not use the LogicPak™ until the problem is corrected.
- Adjustment location--tells which potentiometer to adjust if a measurement is out of range.
- Comments--gives special instructions for particular tests.

The DC calibration procedures follow:

CAUTION

Remove all devices from the sockets before entering the calibration mode (see section 3.4.3 for details). Calibration voltages may damage any device in the LogicPak™ sockets.

1. Turn the programmer power on.
2. Put the programmer into the calibration mode by following the key sequences in table 4-1. The table also explains how to increment, decrement step 2, and how to enter calibration at an advanced step (which is required during the waveform calibration part of the process).
3. Perform the general calibration steps (steps 1-10 and 16) on the measurement chart.

Table 4-1. Key Sequence to Access the Calibration Mode

Programmer System	Key Sequence to Enter Calibration Mode	Increment Step No.	Decrement Step No.
19	Press SELECT Press C2 Press ENTER Enter Step Number [a] Press START	Enter	Review
29A	Press SELECT Press C1 Press START Enter Stem Number [a] Press START	Start	Review
100A	Press SELECT Press 12 Enter Step Number [a] Press START	Start	Backspace

[a] Optional

CAUTION

If the LogicPak™ fails the second step on the measurement chart, DO NOT proceed to the next step. The hardware must pass this step or further testing may damage the LogicPak™.

If the LogicPak™ fails any step on the measurement chart, do not continue to the next step. Refer to table 4-2, which lists error codes and descriptions. Subsequent tests will not give valid results unless all preceding steps are passed and adjustments made.

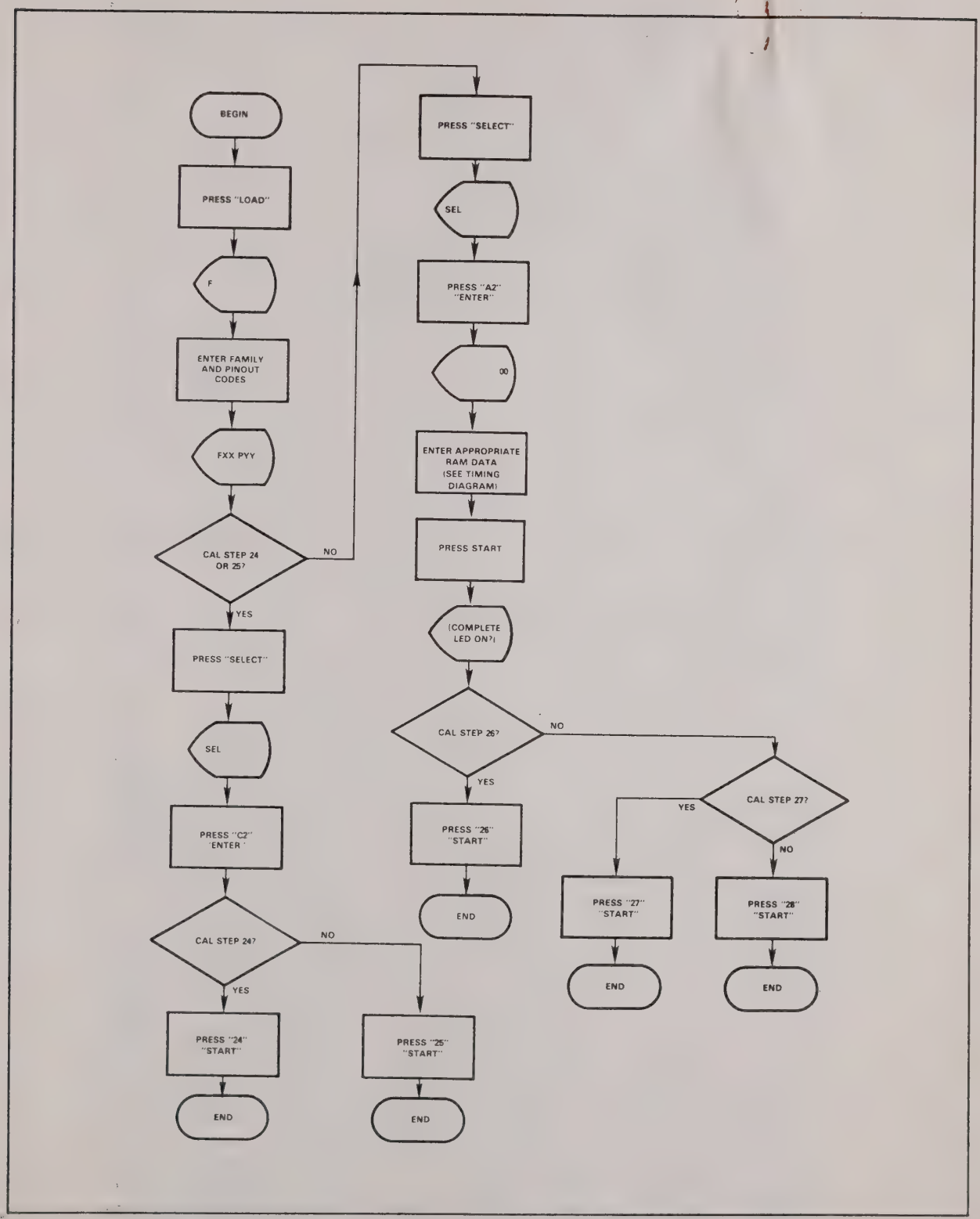


Figure 4-9. Accessing Calibration Steps 24, 25, 26, 27, and 28 (System 19)

REVISIONS

LTR	DESCRIPTION	P.E	DATE
A	Release	[illegible]	4/28/83

Table 4-3. Measurement Chart for MMI National PAL® Adapter (continued)

10-715-1965 (303A-002)

STEP	TEST NO.	TEST DESCRIPTION	MEASUREMENT LOCATION Socket/pins or circuit board test points	MEASUREMENT MIN	MEASUREMENT NOM	MEASUREMENT MAX	ADJUSTMENT LOCATION	COMMENTS Ground pin 10 to 12[a]
	18		20 pin/pins 2,4,6,8,11,13,15,17,19	3.0		5.2		
7	19	Socket pins source	24 pin/pins 1,3,5,7,9,11,15,17,20,22	9.5	--	10.5		
			20 pin/pins 1,3,5,7,9,12,14,16,18	9.5		10.5		
8	20	Backwards device test	24 pin/pin 24 20 pin/pin 20					CAUTION[b,c]
								Load with 10Ω to ground, confirm
								error 32.
9	21	Overcurrent test						CAUTION[c]
		Low range V_{CC}	24 pin/pin 24 20 pin/pin 20					Load with 20Ω 5W to ground,
								confirm error 31.
		Low range CE switch	24 pin/pin 13					Load with 30Ω 5W to ground,
								confirm error 31.
		Low range bit switch 1	24 pin/pin 19					Load with 30Ω 5W to ground,
								confirm error 31.
		Low range bit switch 2	24 pin/pin 14					Load with 30Ω 5W to ground,
								confirm error 31.
								CAUTION[c]
10	22	Overcurrent test						Same loads as step 9, confirm no
		High range	24 pin/pin 24 20 pin/pin 20					errors.

[a]Connect the ground of the DVM to ground pin 10 on a 20-pin socket, to pin 12 on a 24-pin socket, or to pin 14 on a 28-pin socket.
[b]Cannot increment to this step or beyond; must enter calibration at an advanced step. (See table 4-2.)
[c]Insert load resistor after pressing START; remove immediately after performing test.

REVISIONS

LTR	DESCRIPTION	P.E.	DATE
A	Release	KM	4/24/85

Table 4-3. Measurement Chart for MMI National PAL® Adapter (continued)

10-715-1965 (303A-002)

STEP	TEST NO.	TEST DESCRIPTION	MEASUREMENT LOCATION Socket/pins or circuit board test points	MEASUREMENT MIN	MEASUREMENT NOM	MEASUREMENT MAX	ADJUSTMENT LOCATION	COMMENTS Ground pin 10 or 12[a]
4	10	Self-test source drivers						See table 4-4 if errors result.
								Possible errors are E0-FF.
	11	LED test 2						Confirm that 20-pin socket
								LED is on and 24-pin LED is off.
	12	Socket pins TTL high	24 pin/pins 2,4,6,8,10,13,16,18,19,21,23	3.0		5.2		
			20 pin/pins 2,4,6,8,11,13,15,17,19	3.0		5.2		
	13	Socket pins TTL low	24 pin/pins 1,3,5,7,9,11,14,15,17,20,22	-0.4		0.8		
			20 pin/pins 1,3,5,7,9,12,14,16,18	-0.4		0.8		
5	14	Socket pins TTL low	24 pin/pins 2,4,6,8,10,13,16,18,19,21,23	-0.4		0.8		
			20 pin/pins 2,4,6,8,11,13,15,17,19	-0.4		0.8		If error 76 occurs during steps
	15	Socket pins TTL high	24 pin/pins 1,3,5,7,9,11,14,15,17,20,22	3.0		5.2		5-16, perform steps 2 and/or 4
			20 pin/pins 1,3,5,7,9,12,14,16,18	3.0		5.2		for diagnostics.
6	16	Socket pins source	24 pin/pins 2,4,6,8,10,13,14,16,18,19,	9.5		10.5		
			21,23	9.5		10.5		
			20 pin/pins 2,4,6,8,11,13,15,17,19	9.5		10.5		
	17	Socket pins TTL high	24 pin/pins 1,3,5,7,9,11,15,17,20,22	3.0		5.2		
			20 pin/pins 1,3,5,7,9,12,14,16,18	3.0		5.2		
7	18	Socket pins TTL high	24 pin/pins 2,4,6,8,10,13,14,16,18,19,	3.0		5.2		
			21,23	3.0		5.2		

[a]Connect the ground of the DVM to ground pin 10 on a 20-pin socket, to pin 12 on a 24-pin socket, or to pin 14 on a 28-pin socket.

REVISIONS

LTR	DESCRIPTION	P.E	DATE
A	Release	HCMM	4/28/83

Table 4-3. Measurement Chart for MMI National PAL® Adapter (continued)

10-715-1965 (303A-002)

STEP	TEST NO.	TEST DESCRIPTION	MEASUREMENT LOCATION Socket/pins or circuit board test points	MEASUREMENT MIN	MEASUREMENT NOM	MEASUREMENT MAX	ADJUSTMENT LOCATION	COMMENTS Ground pin 10 to 12[a]
	18		20 pin/pins 2,4,6,8,11,13,15,17,19	3.0		5.2		
7	19	Socket pins source	24 pin/pins 1,3,5,7,9,11,15,17,20,22	9.5	--	10.5		
			20 pin/pins 1,3,5,7,9,12,14,16,18	9.5		10.5		
8	20	Backwards device test	24 pin/pin 24 20 pin/pin 20					CAUTION[b,c]
								Load with 10Ω to ground, confirm
								error 32.
9	21	Overcurrent test						CAUTION[c]
		Low range V_{CC}	24 pin/pin 24 20 pin/pin 20					Load with 20Ω 5W to ground,
								confirm error 31.
		Low range CE switch	24 pin/pin 13					Load with 30Ω 5W to ground,
								confirm error 31.
		Low range bit switch 1	24 pin/pin 19					Load with 30Ω 5W to ground,
								confirm error 31.
		Low range bit switch 2	24 pin/pin 14					Load with 30Ω 5W to ground,
								confirm error 31.
								CAUTION[c]
10	22	Overcurrent test						Same loads as step 9, confirm no
		High range	24 pin/pin 24 20 pin/pin 20					errors.

[a]Connect the ground of the DVM to ground pin 10 on a 20-pin socket, to pin 12 on a 24-pin socket, or to pin 14 on a 28-pin socket.
[b]Cannot increment to this step or beyond; must enter calibration at an advanced step. (See table 4-2.)
[c]Insert load resistor after pressing START; remove immediately after performing test.

REVISIONS

LTR	DESCRIPTION	P.E	DATE
A	Release	TMM	4/24/81

Table 4-3. Measurement Chart for MMI National PAL® Adapter (continued)

10-715-1965 (303A-002)

STEP	TEST NO.	TEST DESCRIPTION	MEASUREMENT LOCATION Socket/pins or circuit board test points	MEASUREMENT MIN	MEASUREMENT NOM	MEASUREMENT MAX	ADJUSTMENT LOCATION	COMMENTS Ground pin 10 or 12[a]
			24 pin/pin 13					
			24 pin/pin 19					
			24 pin/pin 14					
	23	High range V_{CC}	24 pin/pin 24 20 pin/pin 20					Load with 5Ω 5W to ground,
								confirm error 31.
10	23	High range CE switch	24 pin/pin 13					Load with 12Ω 5W to ground,
								confirm error 31.
		High range BIT switch 1	24 pin/pin 19					Load with 12Ω 5W to ground,
								confirm error 31.
		High range BIT switch 2	24 pin/pin 14					Load with 12Ω 5W to ground,
								confirm error 31.
11	24	Waveform observation	Refer to timing diagram (this step					Verify waveforms per timing
		for security fuse	number) for test points, family					diagrams.[b]
		programming	pin code, and waveforms.					
12	25	Static programming						Note [b,c]
		Levels VCCP	20 pin/pin 20	11.5		12.0		F 22 P 17
		CE Gen VIHH	20 pin/pin 1	11.5		12.0		Voltages are for fuse 32.
		BIT Gen VIHH	20 pin/pin 19	11.5		12.0		Family code = 95 and 22

[a]Connect the ground of the DVM to ground pin 10 on a 20-pin socket, to pin 12 on a 24-pin socket, or to pin 14 on a 28-pin socket.
[b]A family pin code must be entered or error 30 will be flagged. See the timing diagrams for valid code.
[c]A fuse number must be entered or default to fuse Ø will occur.

REVISIONS

LTR	DESCRIPTION	P E	DATE
A	Release	RMM	4/28/83

Table 4-3. Measurement Chart for MMI National PAL® Adapter (continued)

10-715-1965 (303A-002)

STEP	TEST NO	TEST DESCRIPTION	MEASUREMENT LOCATION Socket/pins or circuit board test points	MEASUREMENT MIN	MEASUREMENT NOM	MEASUREMENT MAX	ADJUSTMENT LOCATION	COMMENTS Ground pin 10 or 12[a]
12	26	Static programming						F 30 P17
		Levels VCCP	20 pin/pin 20	9.75		10.25		Voltages are for fuse 32.
		VIHH	20 pin/pin 1	9.75		10.25		Family code = 30
		VIHH	20 pin/pin 19	9.75		10.25		
13	27	Waveform observation	Refer to timing diagram					Note [b,c]
		Verify array	(this step number) for test points,					Verify waveforms per timing
			family pinout code, and waveforms					diagram for fuse number indicated.
14	28	Waveform observation	Refer to timing diagram					Note[b,c]
		Program array	(this step number) for test points,					Verify waveforms per timing
			family pinout code, and waveforms					diagram for fuse number indicated.
15	29	Waveform observation	No timing diagram supplied; waveforms					Load RAM for desired pattern.
		Program all fuses (opt)	will vary depending on RAM data					Waveforms are for fuses that have
								data stored in RAM.
16	30	Rise time adjust (tr2)						
		CE switch	24 pin/pin 2	9.0uS		11.0uS	R1/701-1941	Adjust R1 for TR2 as shown on
		BIT switch 1	24 pin/pin 23	8.0uS		12.0uS		timing diagram (this step
		BIT switch 2	24 pin/pin 18	8.0uS		12.0uS		number) Load with 100 Ohm, 2W
								5% to GND
17	31	Supply linearity						
		V_{CC} supply	24 pin/pin 24					Verify waveforms per
		CE supply	24 pin/pin 16					timing diagram (this step number).
		BIT supply	24 pin/pin 19					Waveforms should be linear as shown.

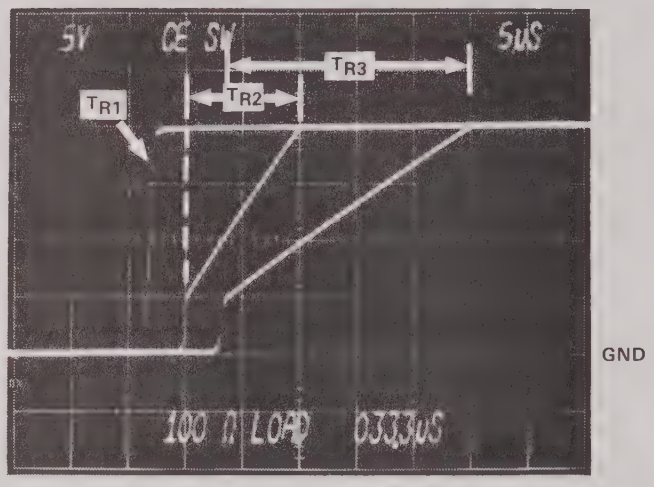
[a]Connect the ground of the DVM to ground pin 10 on a 20-pin socket, to pin 12 on a 24-pin socket, or to pin 14 on a 28-pin socket.
[b]A family pin code must be entered or error 30 will be flagged. See the timing diagrams for valid code.
[c]A fuse number must be entered or default to fuse Ø will occur.
Note: Voltage levels are for calibration purposes only and are not the specified levels of the device manufacturer for manufacturer-specific levels; refer to step 12.

Measurement Chart Photographs

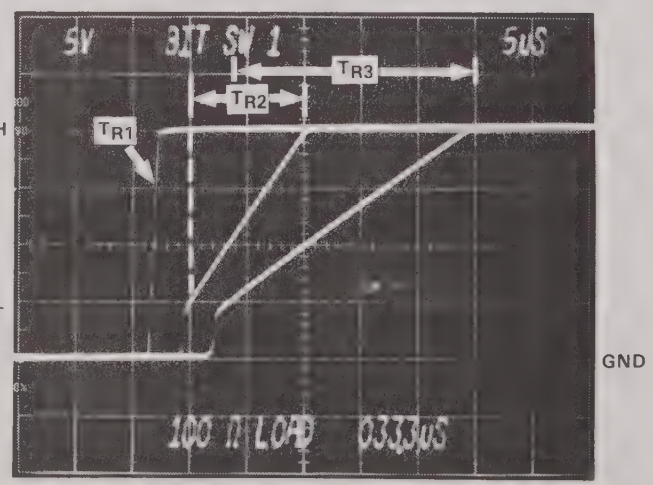
Measurement Chart

PROGRAM ELECTRONICS — RISE TIME WAVEFORM

CHIP ENABLE SWITCH PIN 2

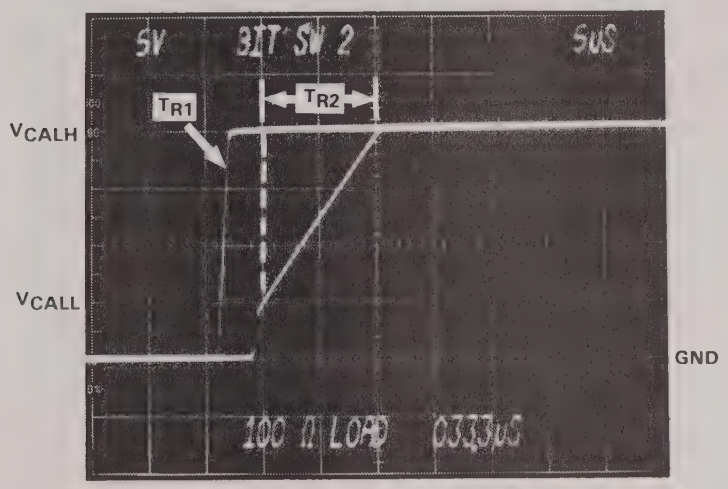


BIT SWITCH 1 PIN 23



DATE	REV	REVISION RECORD	DR	CK

BIT SWITCH 2 PIN 18



SIGNAL CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V_{CALH}	--	20		V	
	V_{CALL}	--	5		V	
	T_{R1} CE SW	.450	.650	.850	us	Adjust R1 on 1941 card for T_{R2} CE SW as shown. Verify that others are within limits. Rise times are measured from V_{CALL} to V_{CALH}. (Voltage levels for reference only).
	T_{R2} CE SW	9.0	10 0	11.0	us	
	T_{R3} CE SW	15.0	20.0	25.0	us	
	T_{R1}BIT SW	450	.650	.850	us	
	T_{R2}BIT SW	8.0	10.0	12 0	us	
	T_{R3}BIT SW	15.0	20.0	25.0	us	

NOTES

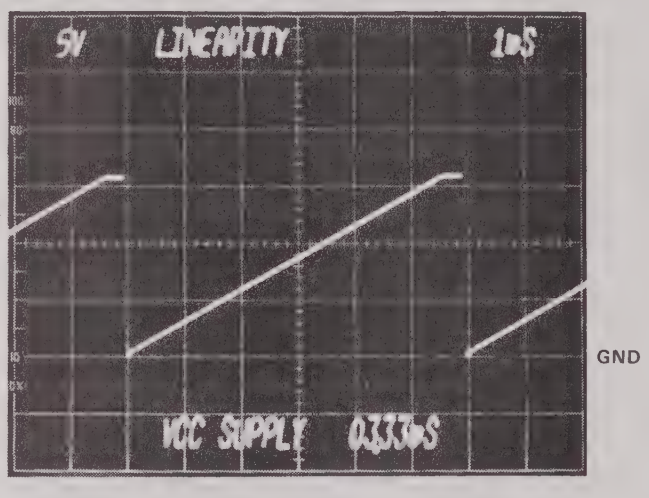
1. *Oscilloscope trigger: TP1 1939 card.*
2. *Step 16 on the measurement chart.*
3. *Test points are for the 24-pin socket.*
4. *BIT SW rise time limits are for both BIT SW1 and BIT SW2.*
5. *All waveforms shown loaded by 100 Ω 2W 5% to ground.*

0526/250/583

Measurement Chart

PROGRAM ELECTRONICS **SUPPLY LINEARITY**

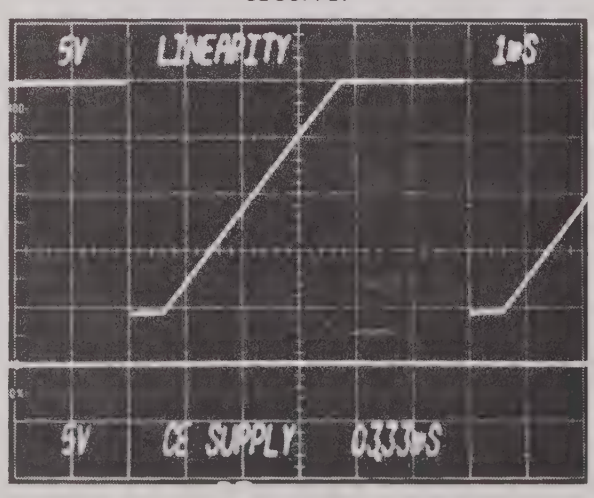
V_{CC} SUPPLY



~ 15 V
PIN 24

GND

CE SUPPLY

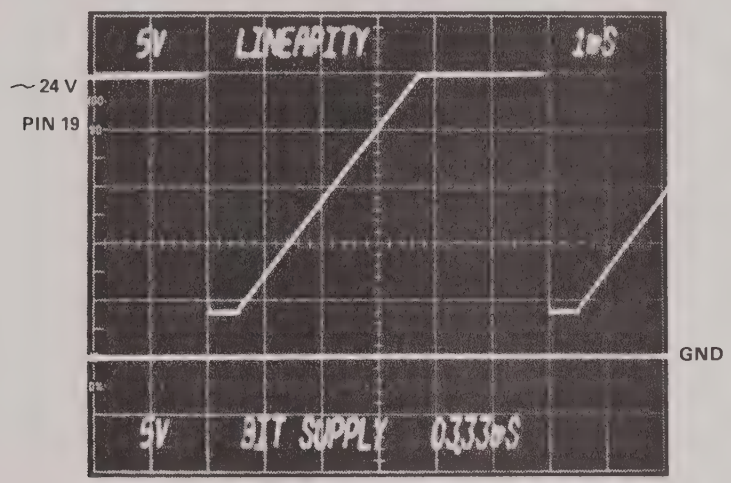


~ 24 V
PIN 6

GND

DATE	REV	REVISION RECORD	DR	CK
	A	Release		

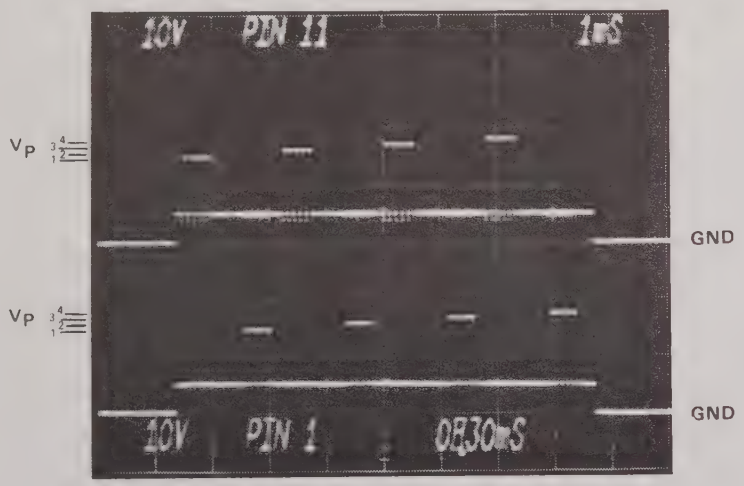
BIT SUPPLY



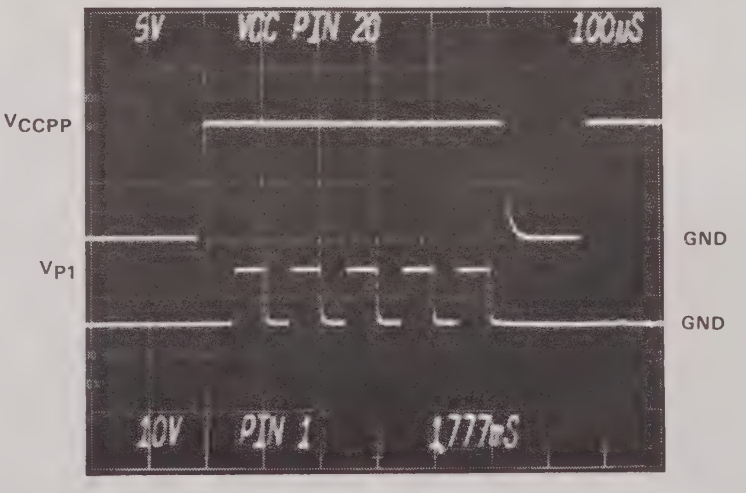
NOTES

1. *Oscilloscope trigger: TP1 1939 card.*
2. *Step 17 on the measurement chart.*
3. *Test points are for the 24-pin socket.*

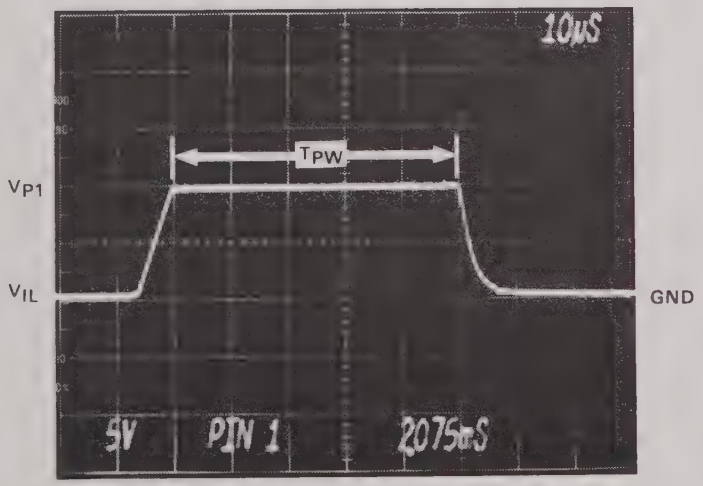
Timing Diagrams


10V PIN 11 1mS
VP
VP
GND
GND
10V PIN 1 0830mS

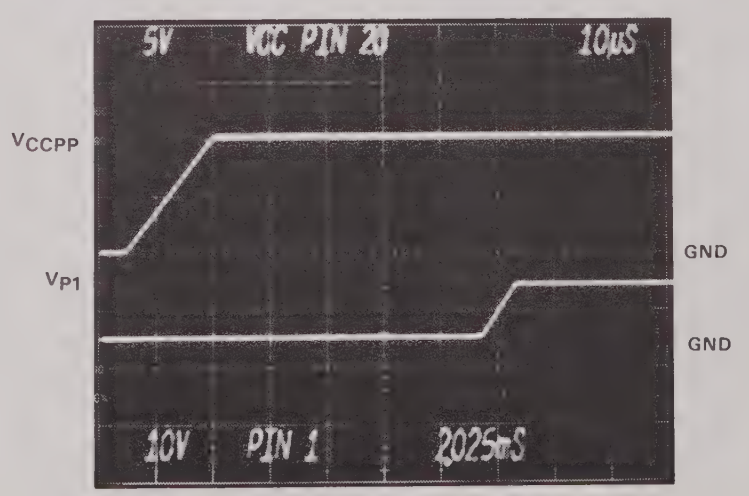
1


5V VCC PIN 20 100uS
VCCPP
VP1
GND
GND
10V PIN 1 1777mS

2


10uS
TPW
VP1
VIL
GND
5V PIN 1 2075mS

3


5V VCC PIN 20 10uS
VCCPP
VP1
GND
GND
10V PIN 1 2025mS

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V_{P1}	14.5	15.0	15.5	V	
	V_{P2}	15.5	16.0	16.5	V	
	V_{P3}	16.5	17.0	17.5	V	
	V_{P4}	17.5	18.0	18.5	V	
	V_{CCPP}	9.5	10.0	10.5	V	
	V_{IL}	-0.4	--	0.8	V	
	T_{PW}	40	50	60	us	(5 Pulses)

NOTES

1. *Oscilloscope trigger: TP1 1939 card.*
2. *Calibration step 11.*
3. *Family pin code 2217.*
4. *Test points are for the 20-pin socket.*
5. *Test points are identified on left side of photos.*
6. *Important pulse widths (T_{PW}) and/or rise times (T_R) are identified on photos.*
7. *Oscilloscope horiz. time base setting is identified on top of photos when delayed sweep is used, the delay time from trigger is on bottom.*
8. *Oscilloscope vert. voltage settings are identified on photos.*

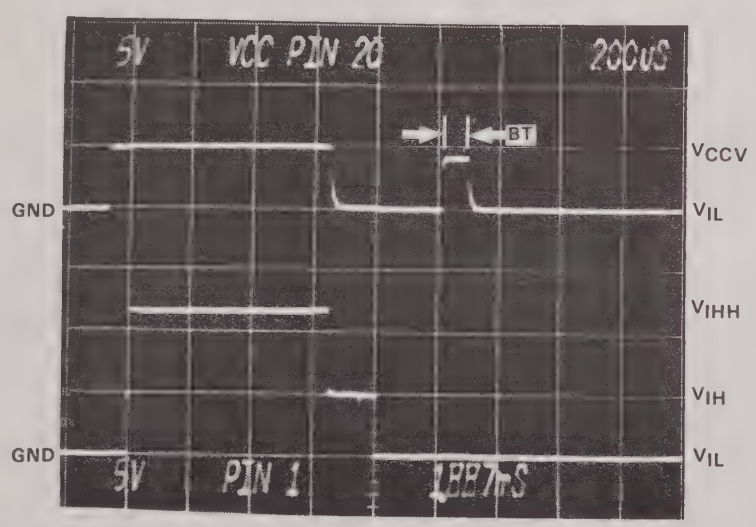
REVISIONS

LTR	DESCRIPTION	P.E.	DATE

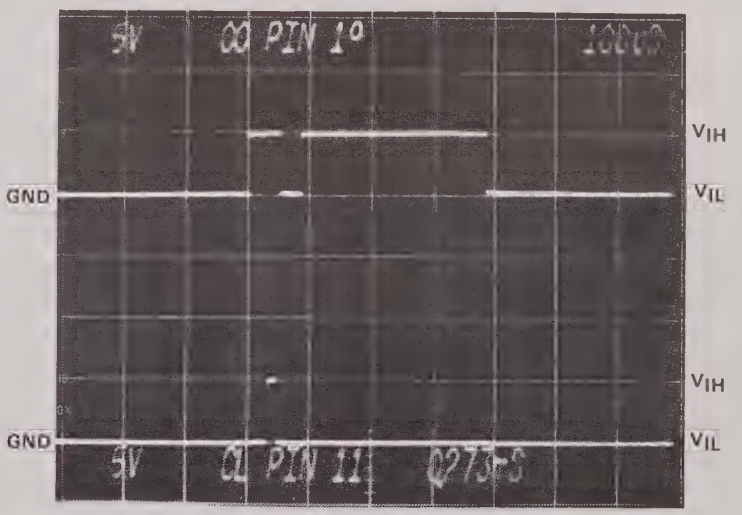
MMI/NATIONAL ADAPTER
LOGICPAK ™ TIMING DIAGRAMS
DEVICE CODE 2217/3017

DATA I/O

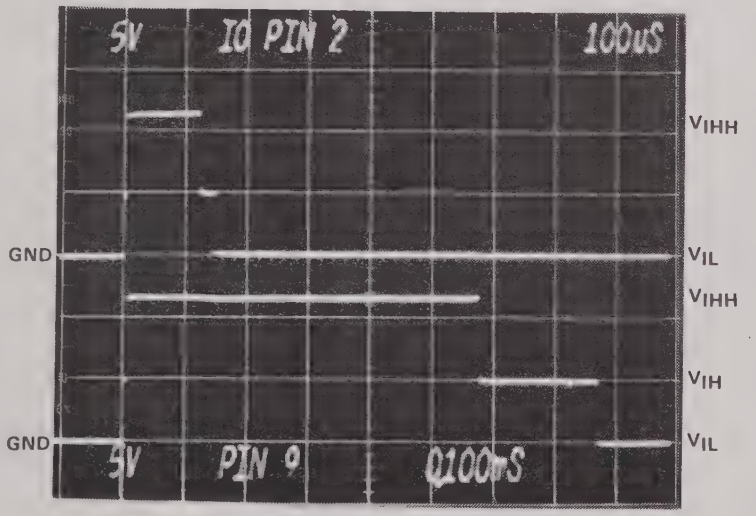
0526/1282


5V
VCC PIN 20
200uS
BT
VCCV
GND
VIL
VIHH
VIH
GND
VIL
5V
PIN 1

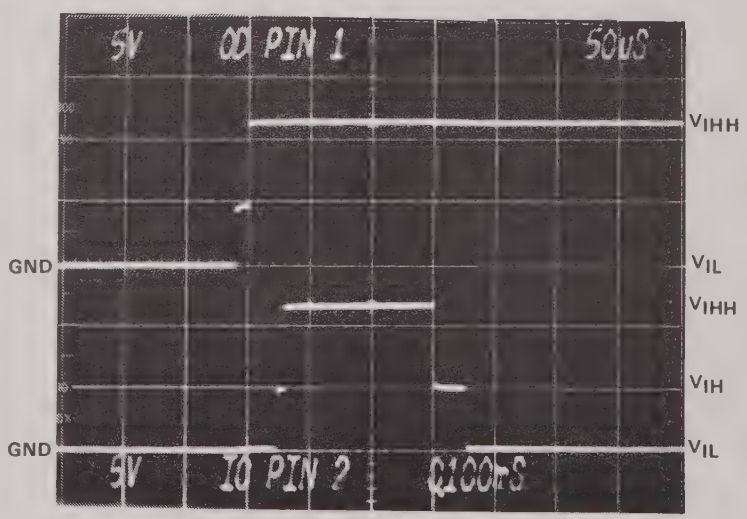
1


5V
VIH
GND
VIL
VIH
GND
VIL

2


5V
IO PIN 2
100uS
VIHH
GND
VIL
VIHH
VIH
GND
VIL
5V
PIN 9

3


5V
OO PIN 1
50uS
VIHH
GND
VIL
VIHH
VIH
GND
VIL
5V
IO PIN 2

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V_{IHH}	11.5	11.75	12.0	V	
	V_{IH}	3.0	--	5.2	V	
	V_{IL}	--	--	0.8	V	
	V_{CCV}	4.75	5.00	5.25	V	
	BT	--	--	--	--	Backward Device Test

NOTES

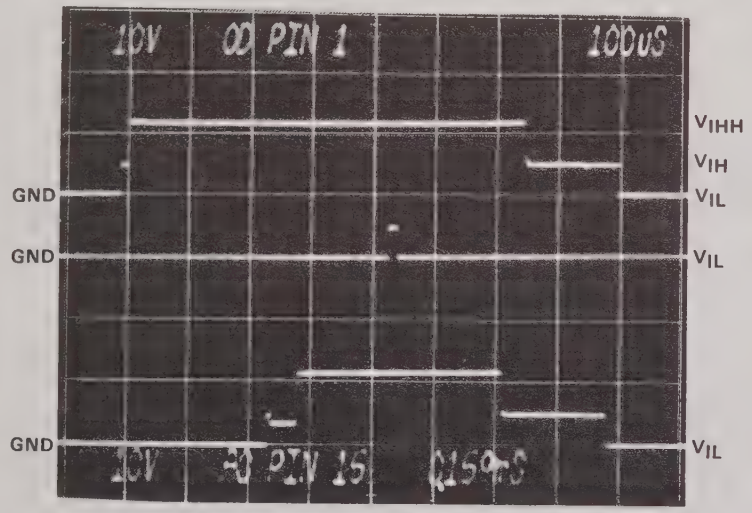
1. *Oscilloscope trigger: TP1 1939 card.*
2. *Calibration step 13.*
3. *Fuse 32.*
4. *Family pin code 2217.*
5. *Test points are for the 20-pin socket.*
6. *Test points are identified on left side of photos.*
7. *Important pulse widths (T_{PW}) and/or rise times (T_R) are identified on photos.*
8. *Oscilloscope horiz. time base setting is identified on top of photos which delayed sweep is used, the delay time from trigger is on bottom.*
9. *Oscilloscope vert. voltage settings are identified on photos.*

REVISIONS

LTR	DESCRIPTION	P.E.	DATE
A	Release	KM	4/29/83

MMI/NATIONAL ADAPTER
LOGICPAK™ TIMING DIAGRAMS
DEVICE CODE 2217/3017

DATA I/O



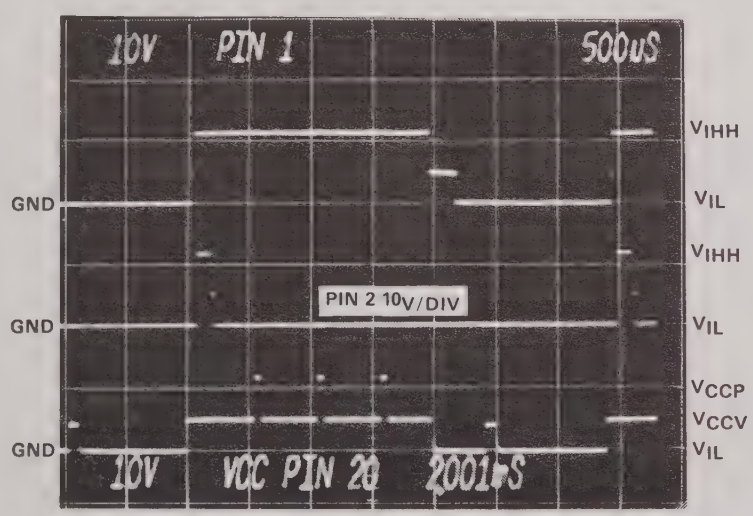
5

4-27
10-715-1965

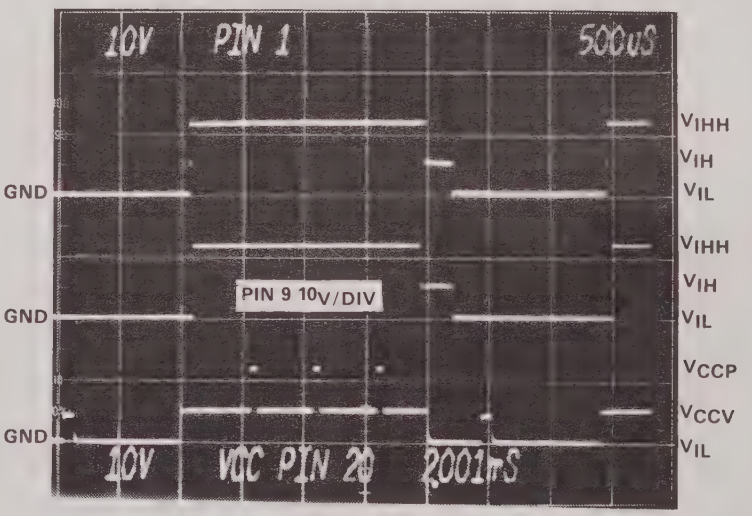
REVISIONS

LTR	DESCRIPTION	P.E.	DATE
		KM	4/29/83

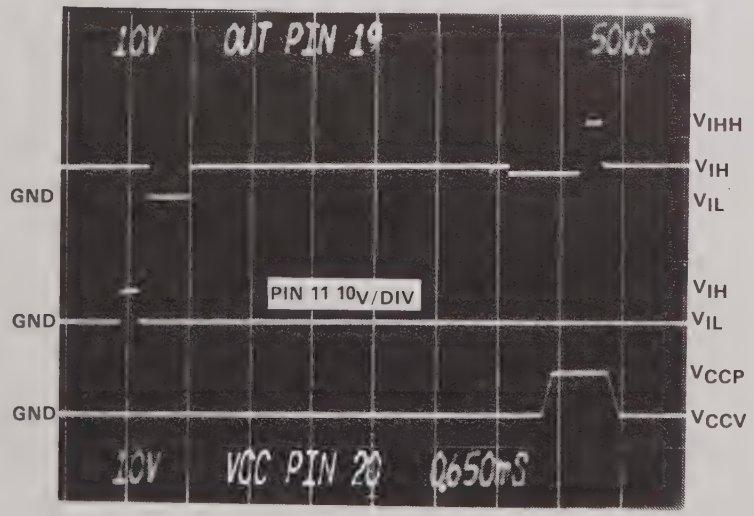
DATA I/O


10V PIN 1 500uS
VIHH
GND
VIL
VIHH
PIN 2 10V/DIV
GND
VIL
VCCP
VCCV
GND
VIL
10V VCC PIN 20 2001mS

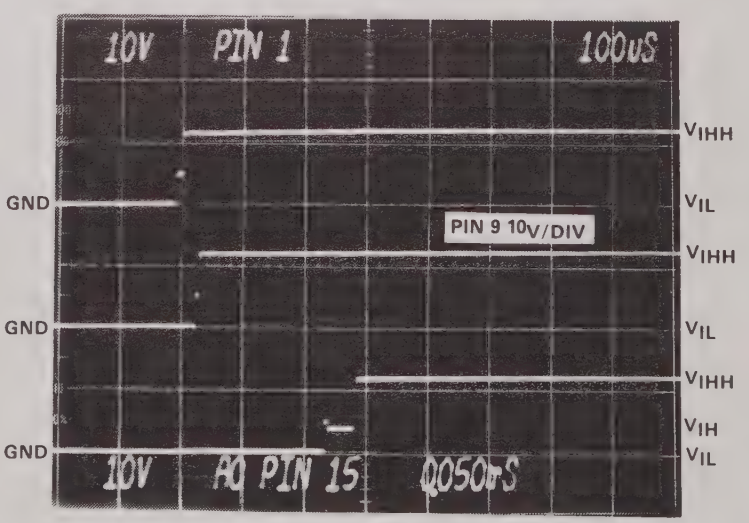
1


10V PIN 1 500uS
VIHH
VIH
GND
VIL
VIHH
PIN 9 10V/DIV
VIH
GND
VIL
VCCP
VCCV
GND
VIL
10V VCC PIN 20 2001mS

2


10V OUT PIN 19 50uS
VIHH
GND
VIH
VIL
PIN 11 10V/DIV
VIH
GND
VIL
VCCP
GND
VCCV
10V VCC PIN 20 0650mS

3


10V PIN 1 100uS
VIHH
GND
VIL
PIN 9 10V/DIV
VIHH
GND
VIL
VIHH
VIH
GND
VIL
10V AO PIN 15 0050mS

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V_{IHH}	11.5	11.75	12.0	V	family code 22
	V_{IHH}	9.75	10.00	10.25	V	family code 30
	V_{IH}	3.0		5.2	V	
	V_{IL}	-0.4	--	0.8	V	
	V_{CCP}	11.5	11.75	12.0	V	family code 22
	V_{CCP}	9.75	10.00	10.25	V	family code 30
	V_{CCV}	4.75	5.00	5.25	V	
	BT	-	-	--	-	Backward Device Test
	TD	1	--	--	us	
	T_{PW}	10	15	50	us	

NOTES

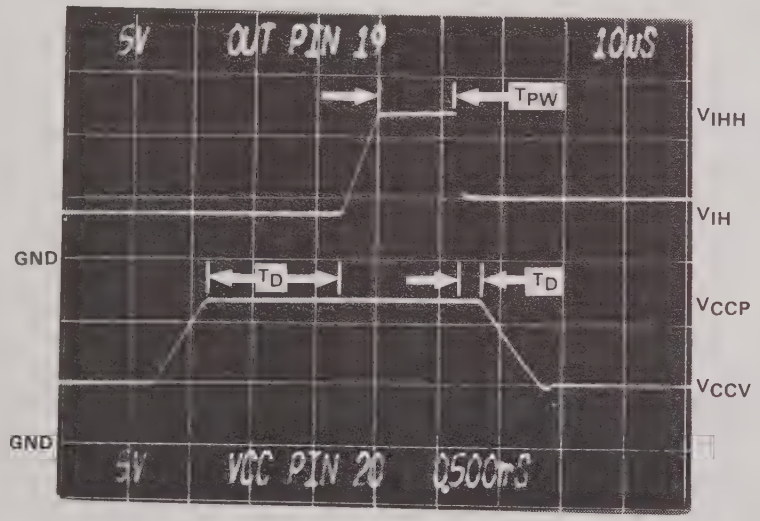
1. *Oscilloscope trigger: TP1 1939 card.*
2. *Calibration step 14.*
3. *Fuse 32.*
4. *Family pin code 2217.*
5. *Test points are for the 20-pin socket.*

REVISIONS

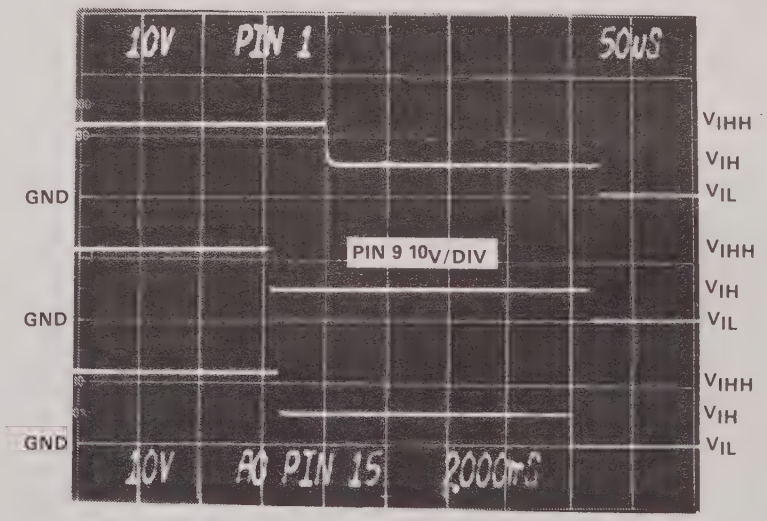
LTR	DESCRIPTION	P.E.	DATE
A	Release	KMM	4/29/83

MMI/NATIONAL ADAPTER
LOGICPAK™ TIMING DIAGRAMS
DEVICE CODE 2217/3017

DATA I/O


5V OUT PIN 19 10uS
T_{PW}
V_{IHH}
V_{IH}
GND
T_D
T_D
V_{CCP}
V_{CCV}
GND
5V VCC PIN 20 0500mS

5

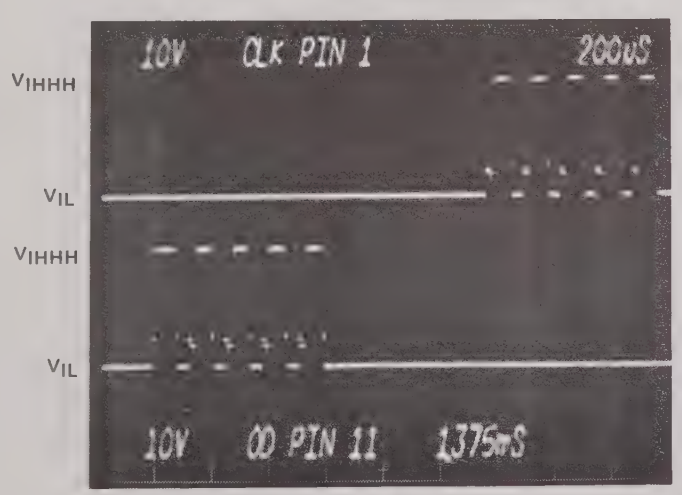

10V PIN 1 50uS
V_{IHH}
V_{IH}
V_{IL}
GND
PIN 9 10V/DIV
V_{IHH}
V_{IH}
GND
V_{IL}
V_{IHH}
V_{IH}
GND
V_{IL}
10V A0 PIN 15 2000mS

6

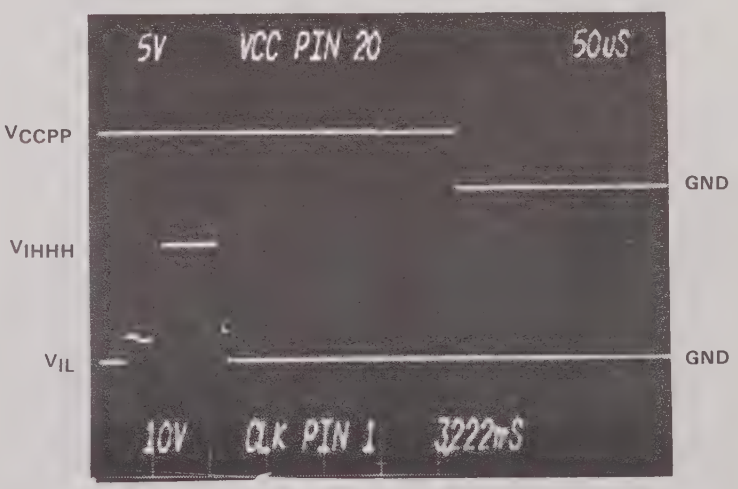
REVISIONS

LTR	DESCRIPTION	P.E.	DATE
		KM	4/29/83

DATA I/O


10V CLK PIN 1 200uS
VIHHH
VIL
VIHHH
VIL
10V OD PIN 11 1375mS

1


5V VCC PIN 20 50uS
VCCPP
GND
VIHHH
VIL
GND
10V CLK PIN 1 3222mS

2

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V_{IL}	-0.4	-	0.8	V	
	V_{IHHH}	19.5	20.0	20.5	V	
	V_{CCPP}	5.25	5.5	5.75	V	

NOTES

1. *Oscilloscope trigger: TP1 1939 card.*
2. *Family/Pinout code 2230.*
3. *Calibration step 11.*
4. *Test points on 20-pin socket.*

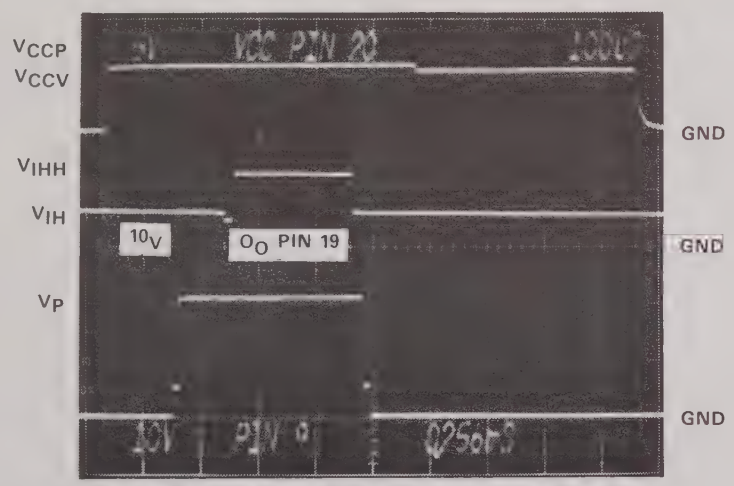
REVISIONS

LTR	DESCRIPTION	P.E.	DATE
A	Release		

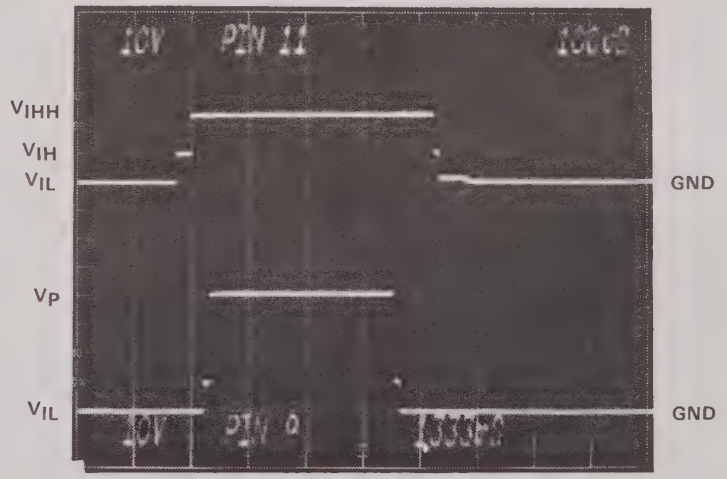
SECURITY FUSE PROGRAMMING WAVEFORMS

FOR FAMILY/PINOUT CODE 2230

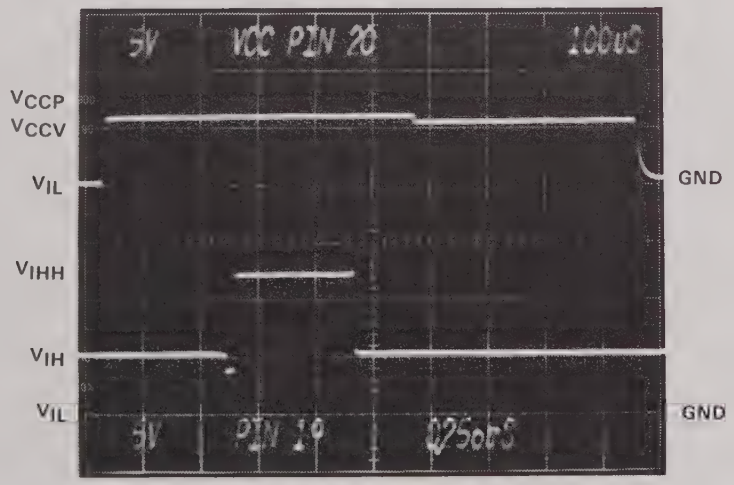
DATA I/O


VCCP
VCCV
VIHH
VIH
VP
GND
GND
GND
10V
PIN 19

1


VIHH
VIH
VIL
VP
VIL
GND
GND

2


5V
VCC PIN 20
100uS
VCCP
VCCV
VIL
VIHH
VIH
VIL
GND
GND
5V
PIN 19

3

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V_{CCP}	5.25	5.50	5.75	V	
	V_{CCV}	4.75	5.00	5.25	V	
	V_{IHH}	11.5	11.75	12.0	V	
	V_{IP}	19.5	20.0	20.5	V	
	V_{IH}	3.0	-	5.2	V	
	V_{IL}	-0.4	-	0.8	V	

NOTES

1. *Oscilloscope trigger: TP1 1939 card.*
2. *Family/Pinout code 2230.*
3. *Calibration step 14.*
4. *Fuse 2048.*
5. *Test points on 20-pin socket.*

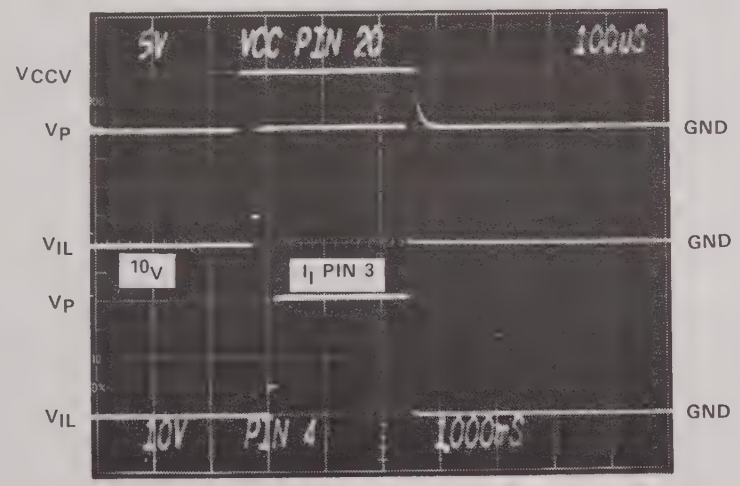
REVISIONS

LTR	DESCRIPTION	P.E.	DATE
A	Release		

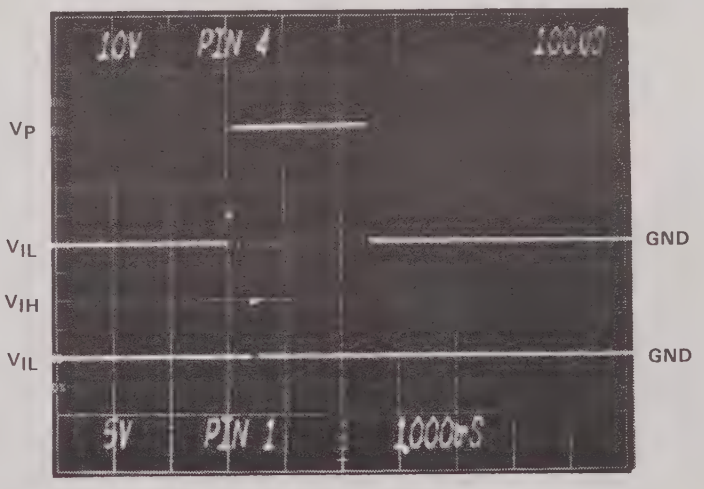
PROGRAMMING WAVEFORMS

FOR FAMILY/PINOUT CODE 2230

DATA I/O


5V
VCC PIN 20
100uS
VCCV
VP
GND
VIL
GND
10V
I1 PIN 3
VP
VIL
GND
10V
PIN 4
1000uS

1


10V
PIN 4
100uS
VP
VIL
GND
VIH
VIL
GND
5V
PIN 1
1000uS

2

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V_{CCV}	4.75	5.00	5.25	V	
	V_P	19.5	20.0	20.5	V	
	V_{IH}	3.0	-	5.2	V	
	V_{IL}	0.4		0.8	V	

NOTES

1. *Oscilloscope trigger: TP1 1939 card.*
2. *Family/Pinout code 2230.*
3. *Calibration step 13.*
4. *Fuse 2048.*
5. *Test points on the 20-pin socket.*

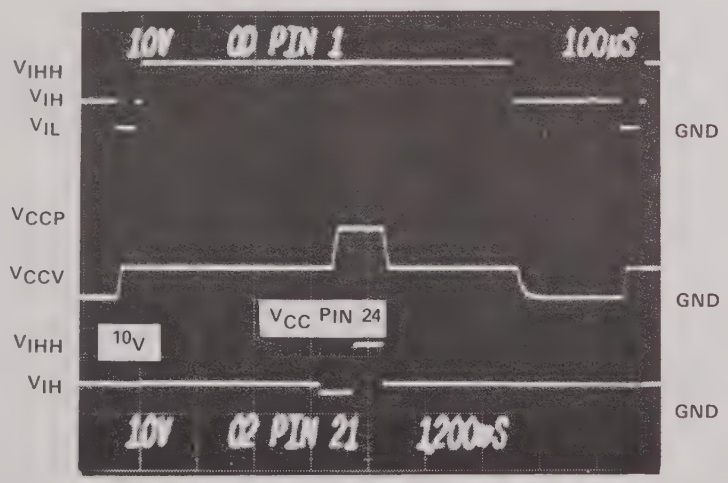
REVISIONS

LTR	DESCRIPTION	P.E.	DATE
A	Release		

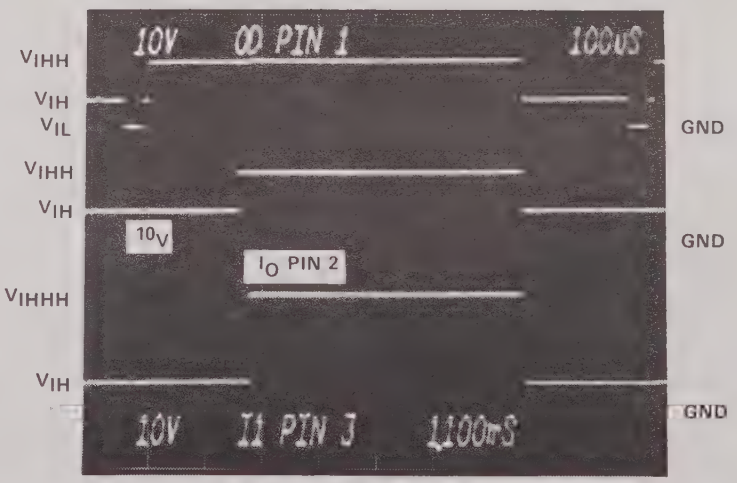
VERIFICATION WAVEFORMS

FOR FAMILY/PINOUT CODE 2230

DATA I/O


10V CO PIN 1 100uS
VIHH
VIH
VIL
GND
VCCP
VCCV
GND
VCC PIN 24
VIHH
10V
VIH
GND
10V O2 PIN 21 1200mS

1


10V CO PIN 1 100uS
VIHH
VIH
VIL
GND
VIHH
VIH
10V
IO PIN 2
GND
VIHHH
VIH
GND
10V I1 PIN 3 1100mS

2

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V_{IL}	0 4		0.8	V	
	V_{IH}	3.0		5.2	V	
	V_{IHH}	11 5	11.75	12.0	V	
	V_{IHHH}	19.5	20.0	20.5	V	
	V_{CCV}					
	V_{CCP}					

NOTES

1. *Oscilloscope trigger: TP1 1939 card.*
2. *Family/Pinout code 2244.*
3. *Fuse 3210.*
4. *Fuse 3210.*
5. *Test points on 24-pin socket.*

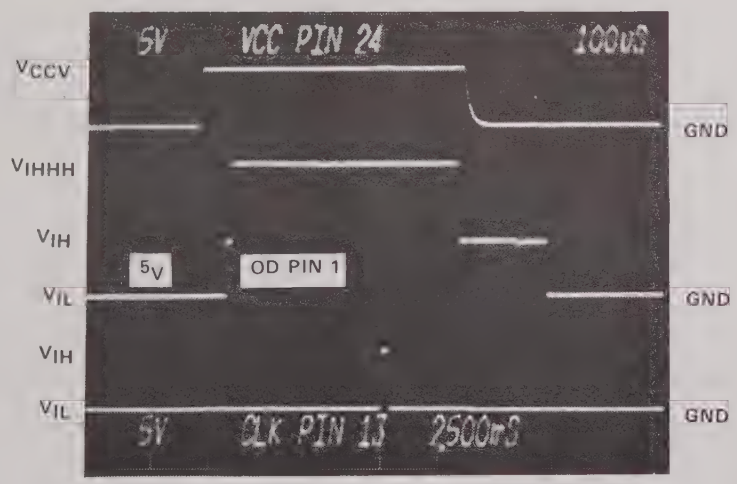
REVISIONS

LTR	DESCRIPTION	P.E.	DATE
A	Release		

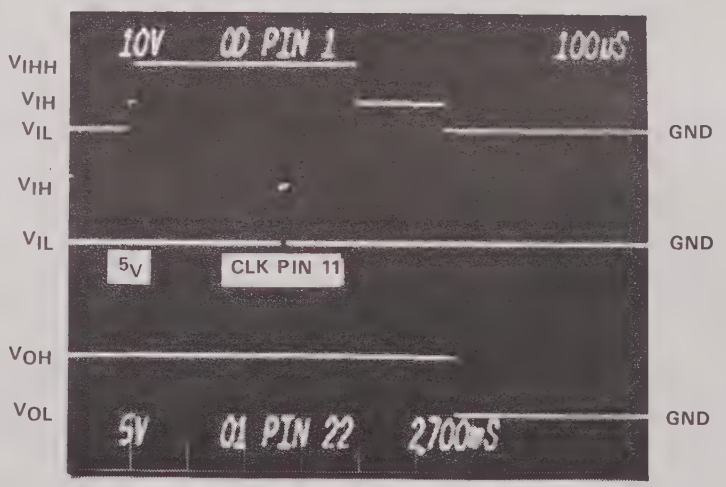
PROGRAMMING WAVEFORMS

FOR FAMILY/PINOUT CODE 2244

DATA I/O


5V VCC PIN 24 100uS
VCCV
GND
VIHHH
VIH
5V
OD PIN 1
VIL
GND
VIH
VIL
5V CLK PIN 13 2500mS
GND

1


10V OD PIN 1 100uS
VIHH
VIH
VIL
GND
VIH
VIL
GND
5V
CLK PIN 11
VOH
VOL
5V 01 PIN 22 2700mS
GND

2

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V_{IL}	-0.4	-	0 8	V	
	V_{IH}	3.0	-	5.2	V	
	V_{IHH}	11.5	11.75	12.0	V	
	V_{IHHH}	19 5	20.0	20.5	V	
	V_{CCV}	4 75	5 0	5.25	V	

NOTES

1. *Oscilloscope trigger: TP1 1939 card.*
2. *Family/Pinout code 2244.*
3. *Calibration step 13.*
4. *Fuse 3210.*
5. *Test points on 24-pin socket.*

REVISIONS

LTR	DESCRIPTION	P.E.	DATE
A	Release		

VERIFICATION WAVEFORMS

FOR FAMILY/PINOUT CODE 2244

DATA I/O

Table 4-4. Error Codes for Calibration

ERROR	I/O PIN[a]	CONDITION	ERROR	I/O PIN[a]	CONDITION
A0	1	Failure to read desired level on input register	D0	17	Failure to read desired TTL level on output pin
A1	2		D1	18	
A2	3		D2	19	
A3	4		D3	20	
A4	5		D4	21	
A5	6		D5	22	
A6	7		D6	23	
A7	8		D7	24	
A8	9		D8	25	
A9	10		D9	26	
AA	11		DA	27	
AB	12		DB	28	
AC	13		DC	29	
AD	14		DD	30	
AE	15		DE	31	
AF	16		DF	32	
BO	17	Failure to read desired level on input register	E0	1	Failure to read desired 10V level on desired output pin
B1	18		E1	2	
B2	19		E2	3	
B3	20		E3	4	
B4	21		E4	5	
B5	22		E5	6	
B6	23		E6	7	
B7	24		E7	8	
B8	25		E8	9	
B9	26		E9	10	
BA	27		EA	11	
BB	28		EB	12	
BC	29		EC	13	
BD	30		ED	14	
BE	31		EE	15	
BF	32		EF	16	
C0	1	Failure to read desired TTL level on output pin	F0	17	Failure to read desired 10V level on desired output pin
C1	2		F1	18	
C2	3		F2	19	
C3	4		F3	20	
C4	5		F4	21	
C5	6		F5	22	
C6	7		F6	23	
C7	8		F7	24	
C8	9		F8	25	
C9	10		F9	--	
CA	11		FA	27	
CB	12		FB	28	
CC	13		FC	--	
CD	14		FD	--	
CE	15		FE	--	
CF	16		FF	--	

[a]See LogicPak™ manual for locations of I/O pins.

SECTION 5

CIRCUIT DESCRIPTION

5.1 INTRODUCTION

This section defines the functions of the 303A-002 MMI/National P/T adapter's principal components. The circuit board assembly is depicted by a block diagram accompanied by a written description.

5.2 GENERAL ARCHITECTURE

The adapter interfaces with the LogicPak™. When it is installed, it customizes the PLDS to support MMI/National logic devices.

5.3 COMPONENT LAYOUT

A block diagram is shown in figure 5-1, and the schematic is at the back of this manual. The adapter board routes all the necessary signals required to perform fuse operations and functional tests of the logic devices. These signals are routed to a socket to support the devices. When the socket is enabled by the family and pinout codes, the LED above the socket will light.

A backward test circuit connects to the V_{CC} pin of each socket. The circuitry tests the orientation of the logic device in the socket. If it is incorrect, an error code will be flagged and operation will stop. The test method limits power to the device, thereby preventing damage to it.

Firmware specific to the MMI/National logic is resident in an EPROM, which receives its address and select inputs from the LogicPak™. The PROM outputs are buffered by an octal data gate, whose inputs feed back to the data base within the LogicPak™. Fuse programming, verification, and functional testing algorithms are stored in PROM and are referenced by stored family and device pinout codes.

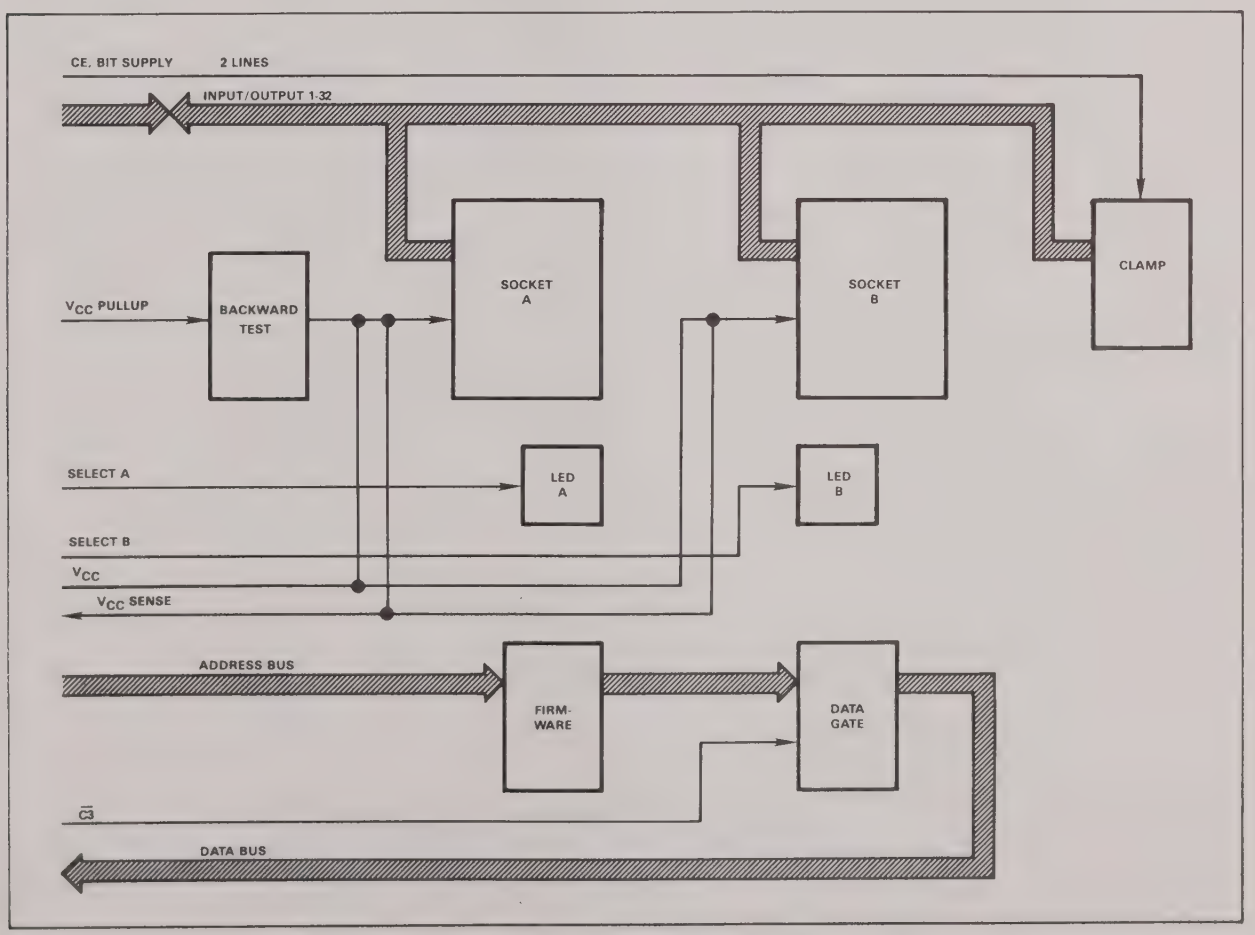


Figure 5-1. Typical Programming/Testing Adapter Block Diagram

APPENDIX A

LOGIC DIAGRAMS
FAMILY AND PINOUT CODES

Table A-1. MMI/National Device Support List

Device	Device Type	No. Pins	Family Pinout	LogicPak	P/T Adapter
Monolithic Memories (MMI)					
6L16A	PAL	24	22/48	V01	303A-002 V08
8L14A	PAL	24	22/49	V01	303A-002 V08
10H8/-2	PAL	20	22/18	V01	303A-002 V08
10L8/-2	PAL	20	22/13	V01	303A-002 V08
12H6/-2	PAL	20	22/19	V01	303A-002 V08
12L6/-2	PAL	20	22/14	V01	303A-002 V08
12L10	PAL	24	22/01	V01	303A-002 V08
14H4/-2	PAL	20	22/20	V01	303A-002 V08
14L4/-2	PAL	20	22/15	V01	303A-002 V08
14L8	PAL	24	22/02	V01	303A-002 V08
16A4	PAL	20	22/24	V01	303A-002 V08
16C1/-2	PAL	20	22/21	V01	303A-002 V08
16H2/-2	PAL	20	22/22	V01	303A-002 V08
16L2/-2	PAL	20	22/16	V01	303A-002 V08
16L6	PAL	24	22/03	V01	303A-002 V08
16L8/A/A-2/A-4	PAL	20	22/17	V01	303A-002 V08
16L8B	PAL	20	30/17	V01	303A-002 V08
16P8A	PAL	20	22/30	V01	303A-002 V08
16R4/A/A-2/A-4	PAL	20	22/24	V01	303A-002 V08
16R4B	PAL	20	30/24	V01	303A-002 V08
16R6	PAL	20	22/24	V01	303A-002 V08
16R6B	PAL	20	30/24	V01	303A-002 V08
16R8	PAL	20	22/24	V01	303A-002 V08
16R8B	PAL	20	30/24	V01	303A-002 V08
16RA8	PAL	20	22/31	V01	303A-002 V08
16RP4A	PAL	20	22/31	V01(2)	303A-002 V08
16RP6A	PAL	20	22/31	V01(2)	303A-002 V08
16RP8A	PAL	20	22/31	V01(2)	303A-002 V08
16R4BP	PAL	20	22/67	V01(2)	303A-002 V08
16R6BP	PAL	20	22/67	V01(2)	303A-002 V08
16R8BP	PAL	20	22/67	V01(2)	303A-002 V08
16X4	PAL	20	22/24	V01	303A-002 V08
18L4	PAL	24	22/04	V01	303A-002 V08
20C1	PAL	24	22/12	V01	303A-002 V08
20L2	PAL	24	22/05	V01	303A-002 V08
20L8/B	PAL	24	22/26	V01	303A-002 V08

Device	Device Type	No. Pins	Family Pinout	LogicPak	P/T Adapter
Monolithic Memories (MMI)					
20L10/B	PAL	24	22/06	V01	303A-002 V08
20R4A/A-2/B	PAL	24	22/27	V01	303A-002 V08
20R6A/A-2	PAL	24	22/27	V01	303A-002 V08
20R4BP	PAL	20	22/68	V01(2)	303A-002 V08
20R6BP	PAL	20	22/68	V01(2)	303A-002 V08
20R8BP	PAL	20	22/68	V01(2)	303A-002 V08
20R8A/A-2/B	PAL	24	22/27	V01	303A-002 V08
20R4B	PAL	24	22/27	V01	303A-002 V08
20R6B	PAL	24	22/27	V01	303A-002 V08
20R8B	PAL	24	22/27	V01	303A-002 V08
20RA10	PAL	24	22/45	V01	303A-002 V08
20RS4	PAL	24	22/46	V01(2)	303A-002 V08
20RS8	PAL	24	22/44	V01(2)	303A-002 V08
20RS10	PAL	24	22/44	V01(2)	303A-002 V08
20S10	PAL	24	22/43	V01	303A-002 V08
20X4	PAL	24	22/23	V01	303A-002 V08
20X4A	PAL	24	22/36	V01(2)	303A-002 V08
20X8	PAL	24	22/23	V01	303A-002 V08
20X8A	PAL	24	22/36	V01(2)	303A-002 V08
20X10	PAL	24	22/23	V01	303A-002 V08
20X10A	PAL	24	22/36	V01(2)	303A-002 V08
National Semiconductor					
10H8/A/A2	PAL	20	95/18	V01	303A-002 V05(1)
10L8/A/A2	PAL	20	95/13	V01	303A-002 V05(1)
12H6/A/A2	PAL	20	95/19	V01	303A-002 V05(1)
12L6/A/A2	PAL	20	95/14	V01	303A-002 V05(1)
12L10	PAL	24	95/01	V01	303A-002 V05(1)
14H4/A/A2	PAL	20	95/20	V01	303A-002 V05(1)
14L4/A/A2	PAL	20	95/15	V01	303A-002 V05(1)
14L8	PAL	24	95/02	V01	303A-002 V05(1)
16C1/A/A2	PAL	20	95/21	V01	303A-002 V05(1)
16H2/A/A2	PAL	20	95/22	V01	303A-002 V05(1)
16L2/A/A2	PAL	20	95/16	V01	303A-002 V05(1)
16L6	PAL	24	95/03	V01	303A-002 V05(1)
16L8/A/A2	PAL	20	95/17	V01	303A-002 V05(1)
16L8B	PAL	20	95/17	V01	303A-002 V08
16R4/A/A2	PAL	20	95/24	V01	303A-002 V05(1)
16R4B	PAL	20	95/24	V01	303A-002 V08

Device	Device Type	No. Pins	Family Pinout	LogicPak	P/T Adapter
National Semiconductor					
16R6/A/A2	PAL	20	95/24	V01	303A-002 V05(1)
16R6B	PAL	20	95/24	V01	303A-002 V08
16R8/A/A2	PAL	20	95/24	V01	303A-002 V05(1)
16R8B	PAL	20	95/24	V01	303A-002 V08
18L4	PAL	24	95/04	V01	303A-002 V05(1)
20C1	PAL	24	95/12	V01	303A-002 V05(1)
20L2	PAL	24	95/05	V01	303A-002 V05(1)
20L8/A	PAL	24	95/26	V01	303A-002 V08
20L10	PAL	24	95/06	V01	303A-002 V05(1)
20R4/A	PAL	24	95/27	V01(2)	303A-002 V08
20R6/A	PAL	24	95/27	V01(2)	303A-002 V08
20R8/A	PAL	24	95/27	V01(2)	303A-002 V08
20X4	PAL	24	95/23	V01	303A-002 V05(1)
20X8	PAL	24	95/23	V01	303A-002 V05(1)
20X10	PAL	24	95/23	V01	303A-002 V05(1)

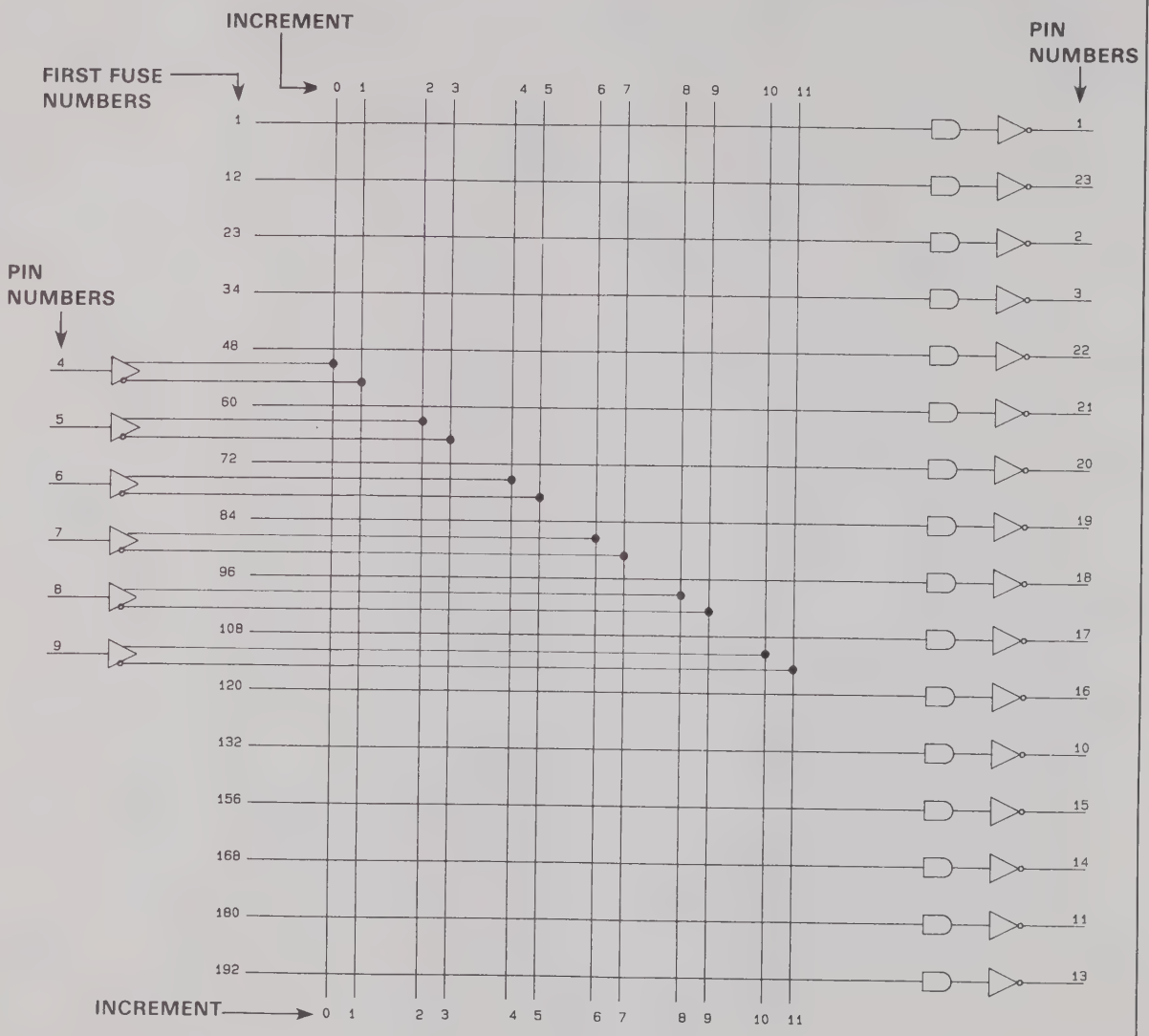
(1) V08 is the preferred version due to some yield improving algorithm changes.
(2) V04 is required for full support of the preload feature.

Table A-1. MMI/National Device Support List

Device	Family Pinout	LogicPak™	P/T Adapter		Adapter	
Monolithic Memories (MMI)						
PAL 6L16	22 48	VO1	303A-002	VO6		
PAL 8L14	22 49	VO1	303A-002	VO6		
PAL 10H8	22 18	VO1	303A-002	VO2	303A-100	VO1
PAL 10L8	22 13	VO1	303A-002	VO2	303A-100	VO1
PAL 12H6	22 19	VO1	303A-002	VO2	303A-100	VO1
PAL 12L6	22 14	VO1	303A-002	VO2	303A-100	VO1
PAL 12L10	22 01	VO1	303A-002	VO2	303A-100	VO1
PAL 14H4	22 20	VO1	303A-002	VO2	303A-100	VO1
PAL 14L4	22 15	VO1	303A-002	VO2	303A-100	VO1
PAL 14L8	22 02	VO1	303A-002	VO1	303A-100	VO1
PAL 16A4	22 24	VO1	303A-002	VO2	303A-100	VO1
PAL 16C1	22 21	VO1	303A-002	VO2	303A-100	VO1
PAL 16H2	22 22	VO1	303A-002	VO2	303A-100	VO1
PAL 16L2	22 16	VO1	303A-002	VO2	303A-100	VO1
PAL 16L6	22 03	VO1	303A-002	VO2	303A-100	VO1
PAL 16L8	22 17	VO1	303A-002	VO2	303A-100	VO1
PAL 16L8B	30 17	VO1	303A-002	VO6	303A-100	VO1
PAL 16P8	22 30	VO1	303A-002	VO5	303A-100	VO3
PAL 16R4	22 24	VO1	303A-002	VO2	303A-100	VO1
PAL 16R4B	30 24	VO1	303A-002	VO6	303A-100	VO1
PAL 16R6	22 24	VO1	303A-002	VO2	303A-100	VO1
PAL 16R6B	30 24	VO1	303A-002	VO6	303A-100	VO1
PAL 16R8	22 24	VO1	303A 002	VO2	303A-100	VO1
PAL 16R8B	30 24	VO1	303A-002	VO6	303A-100	VO1
PAL 16RP4	22 31	VO1+	303A-002	VO5		
PAL 16RP6	22 31	VO1+	303A-002	VO5		
PAL 16RP8	22 31	VO1+	303A-002	VO5		
PAL 16X4	22 24	VO1	303A-002	VO2	303A-100	VO1
PAL 18L4	22 04	VO1	303A-002	VO2	303A-100	VO1
PAL 20C1	22 12	VO1	303A-002	VO2	303A-100	VO1
PAL 20L2	22 05	VO1	303A-002	VO2	303A-100	VO1
PAL 20L8	22 26	VO1	303A-002	VO2	303A-100	VO1
PAL 20L10	22 06	VO1	303A-002	VO2	303A-100	VO1
PAL 20R4	22 27	VO1	303A-002	VO2	303A-100	VO1
PAL 20R6	22 27	VO1	303A-002	VO2	303A-100	VO1
PAL 20R8	22 27	VO1	303A-002	VO2	303A-100	VO1
PAL 20RA10	22 45	VO1	303A-002	VO5		
PAL 20RS4	22 46	VO1+	303A-002	VO5		
PAL 20RS8	22 44	VO1+	303A-002	VO5		
PAL 20RS10	22 44	VO1+	303A-002	VO5		
PAL 20S10	22 43	VO1	303A-002	VO5		
PAL 20X4	22 23	VO1	303A-002	VO2	303A-100	VO1
PAL 20X8	22 23	VO1	303A-002	VO2	303A-100	VO1
PAL 20X10	22 23	VO1	303A-002	VO2	303A-100	VO1
National Semiconductor						
PAL 10H8	95 18	VO1	303A-002	VO5	303A 100	VO1
PAL 10L8	95 13	VO1	303A-002	VO5	303A-100	VO1
PAL 12H6	95 19	VO1	303A-002	VO5	303A-100	VO1
PAL 12L6	95 14	VO1	303A-002	VO5	303A-100	VO1
PAL 12L10	95 01	VO1	303A-002	VO5	303A-100	VO1
PAL 14H4	95 20	VO1	303A-002	VO5	303A-100	VO1
PAL 14L4	95 15	VO1	303A 002	VO5	303A-100	VO1
PAL 14L8	95 02	VO1	303A-002	VO5	303A-100	VO1
PAL 16C1	95 21	VO1	303A-002	VO5	303A-100	VO1
PAL 16H2	95 22	VO1	303A-002	VO5	303A-100	VO1
PAL 16L2	95 16	VO1	303A-002	VO5	303A-100	VO1
PAL 16L6	95 03	VO1	303A-002	VO5	303A-100	VO1
PAL 16L8	95 17	VO1	303A-002	VO5	303A-100	VO1
PAL 16R4	95 24	VO1	303A-002	VO5	303A-100	VO1
PAL 16R6	95 24	VO1	303A-002	VO5	303A-100	VO1
PAL 16R8	95 24	VO1	303A-002	VO5	303A-100	VO1
PAL 18L4	95 04	VO1	303A-002	VO5	303A-100	VO1
PAL 20C1	95 12	VO1	303A-002	VO5	303A-100	VO1
PAL 20L2	95 05	VO1	303A-002	VO5	303A-100	VO1
PAL 20L10	95 06	VO1	303A-002	VO5	303A-100	VO1
PAL 20X4	95 23	VO1	303A-002	VO5	303A-100	VO1
PAL 20X8	95 23	VO1	303A-002	VO5	303A-100	VO1
PAL 20X10	95 23	VO1	303A-002	VO5	303A-100	VO1

+ LogicPak revision VO4 required for full support of device register preload feature.

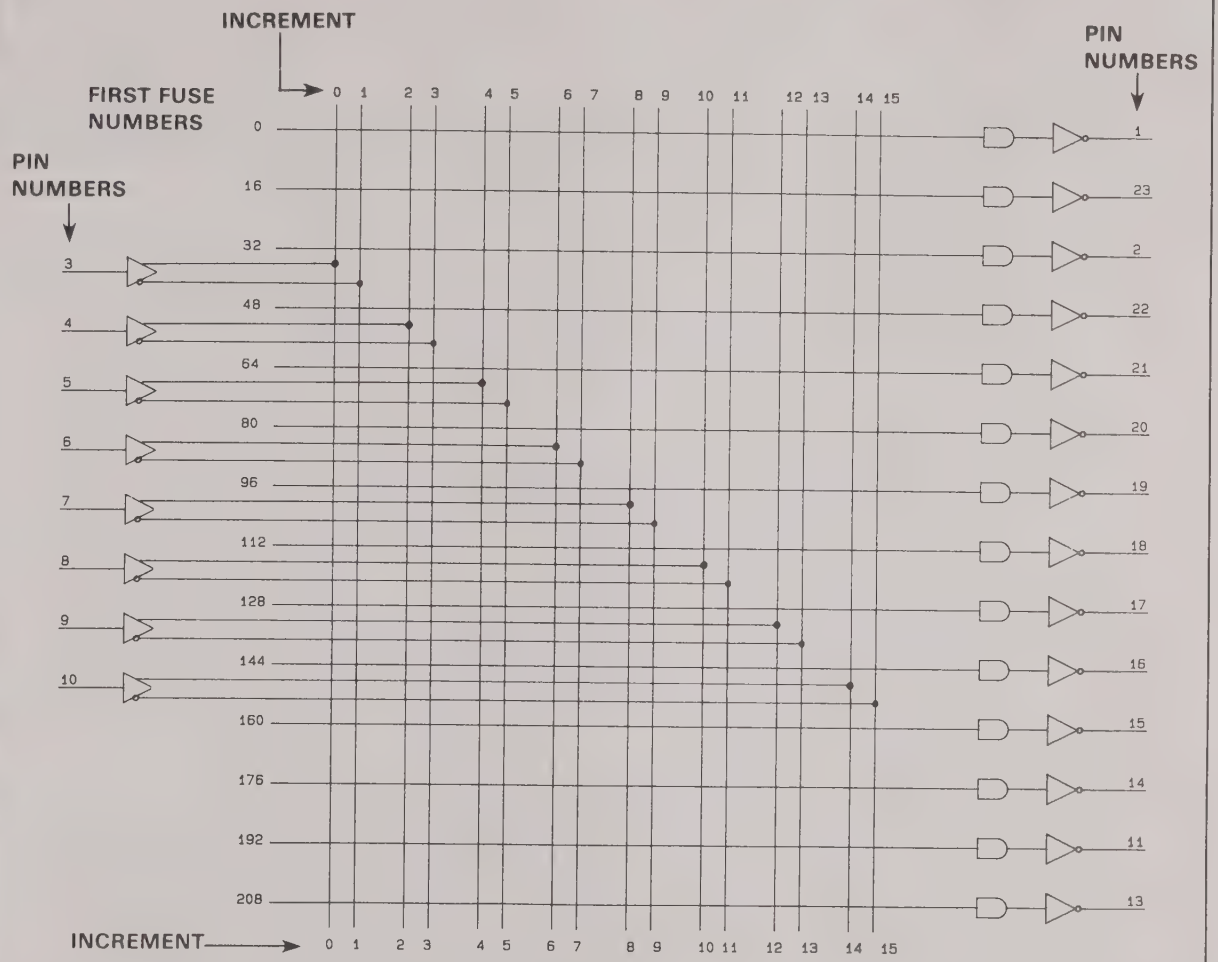
Logic Diagram PAL6L16



NOTE: Fuse Number = First Fuse Number + Increment

Figure A-1. Logic Diagram PAL6L16

Logic Diagram PAL8L14



NOTE: Fuse Number = First Fuse Number + Increment

Figure A-2. Logic Diagram PAL8L14

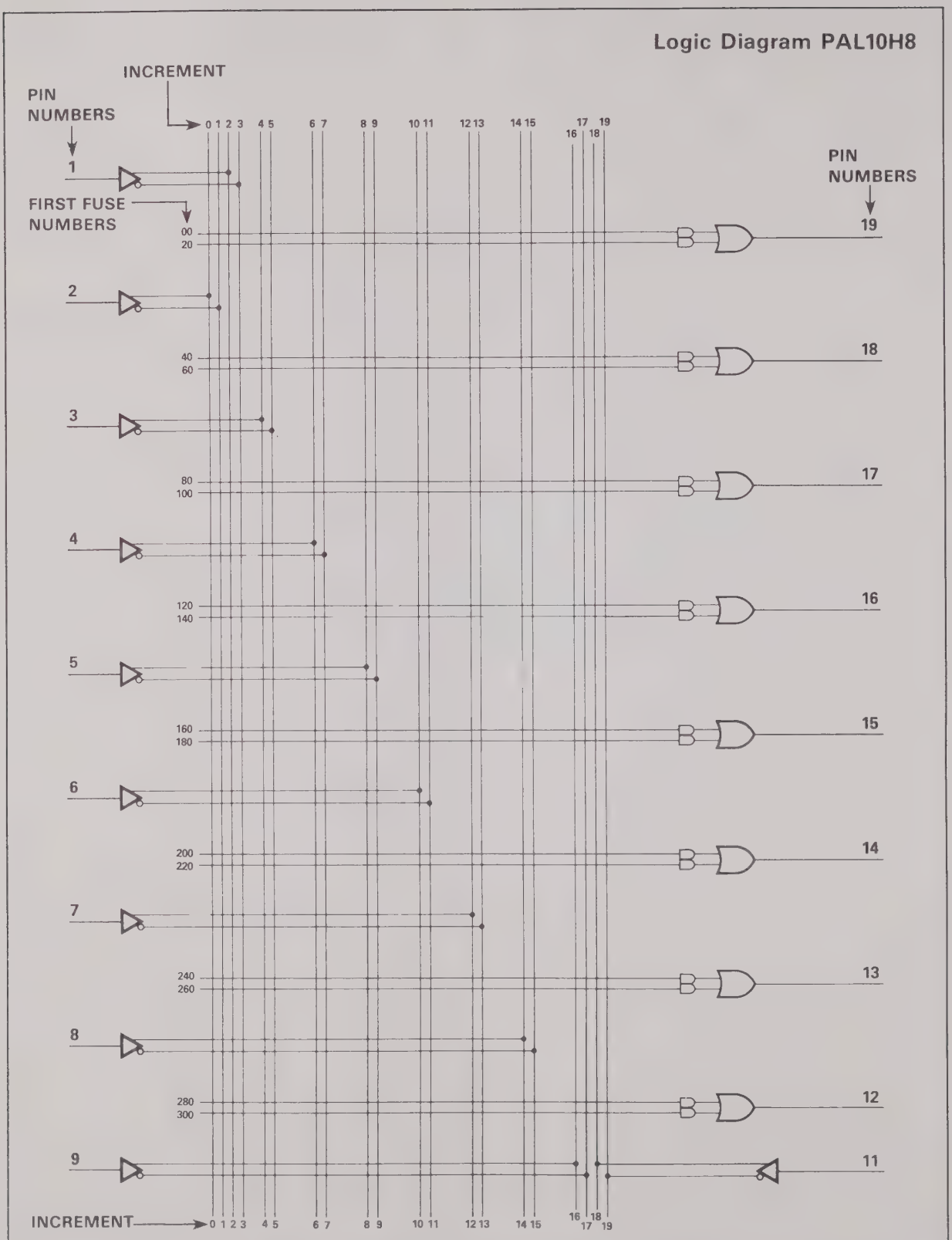
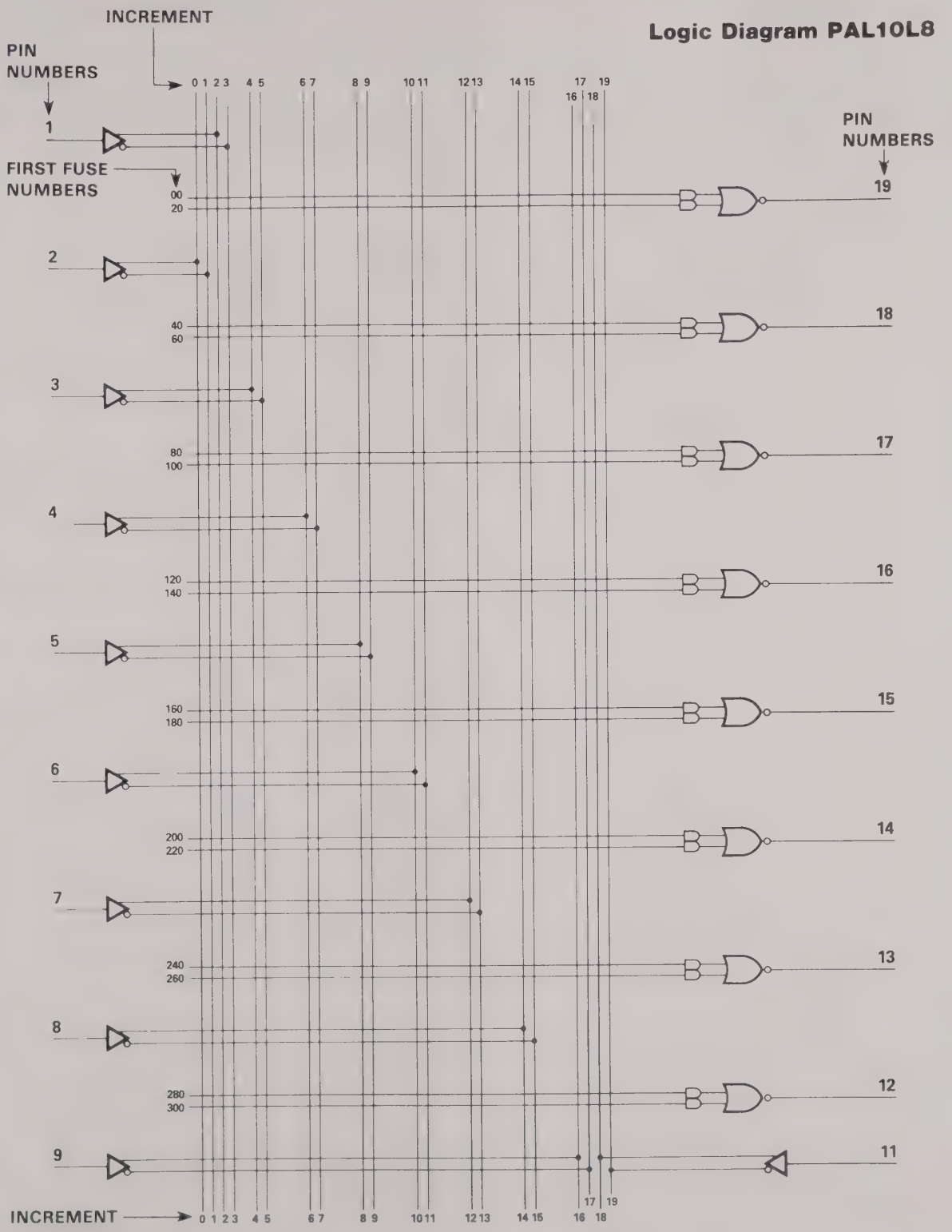


Figure A-3. Logic Diagram PAL10H8



NOTE: Fuse Number = First Fuse Number + Increment

Figure A-4. Logic Diagram PAL10L8

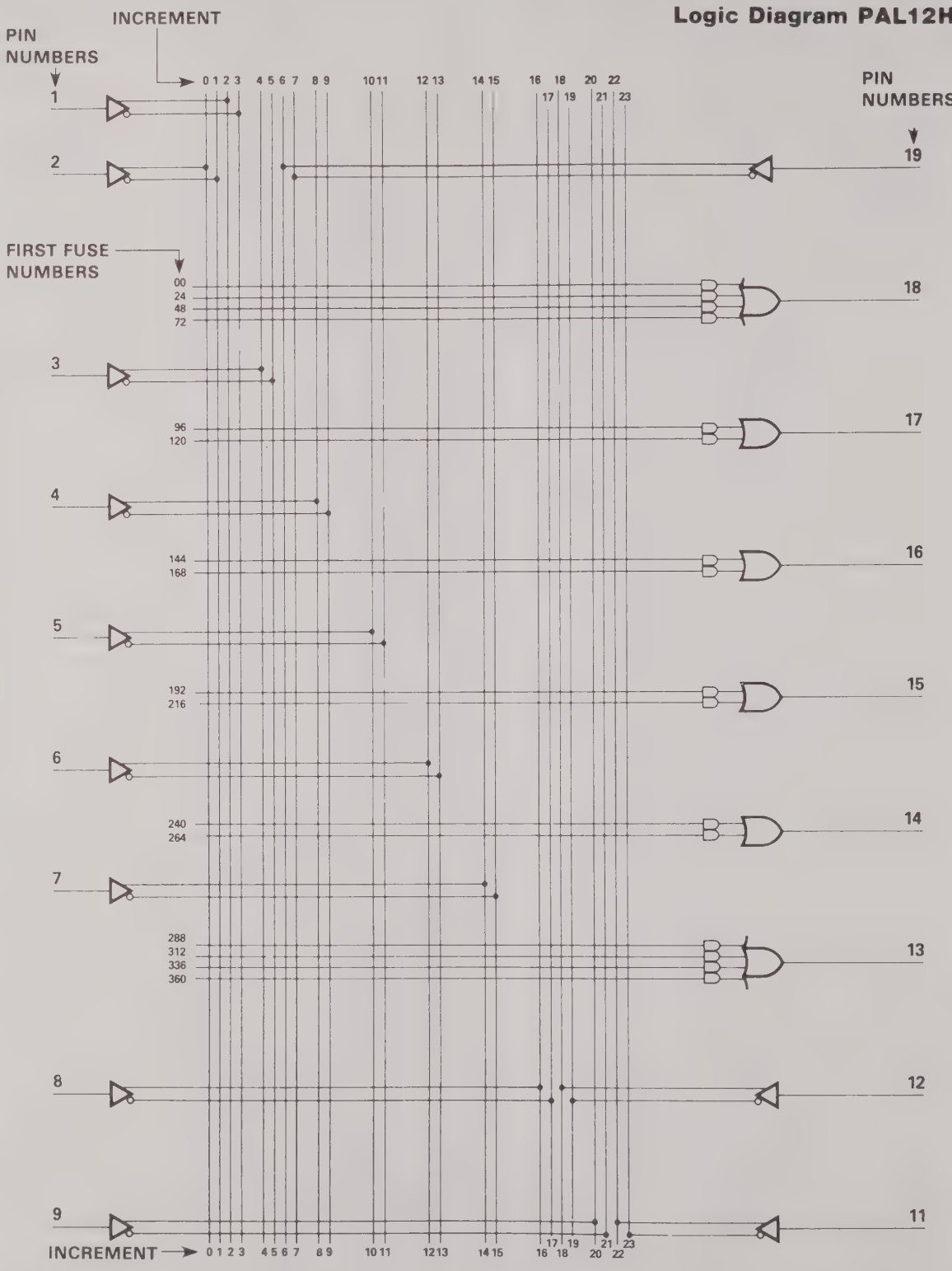
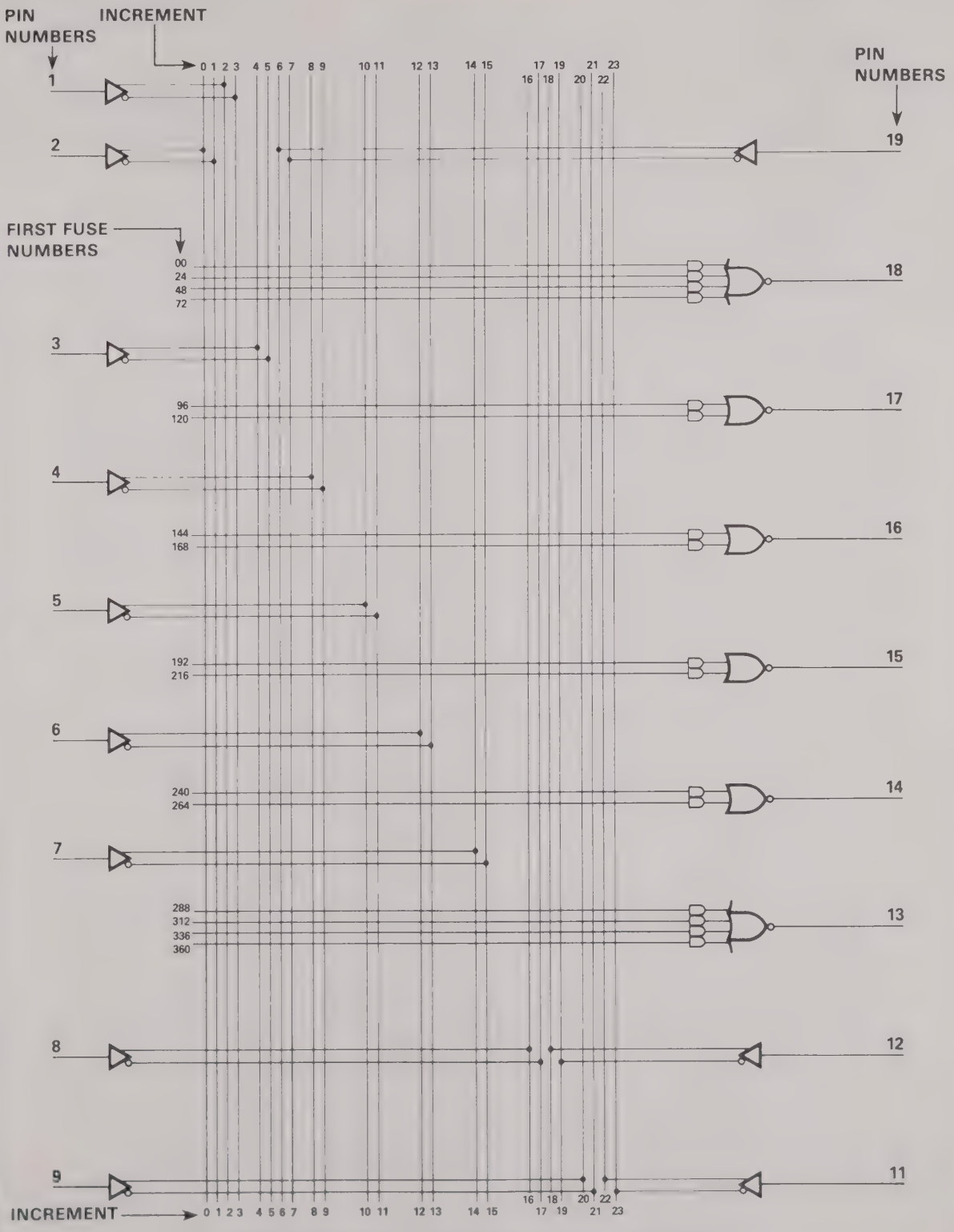


Figure A-5. Logic Diagram PAL12H6

Logic Diagram PAL12L6



NOTE: Fuse Number = First Fuse Number + Increment

Figure A-6. Logic Diagram PAL12L6

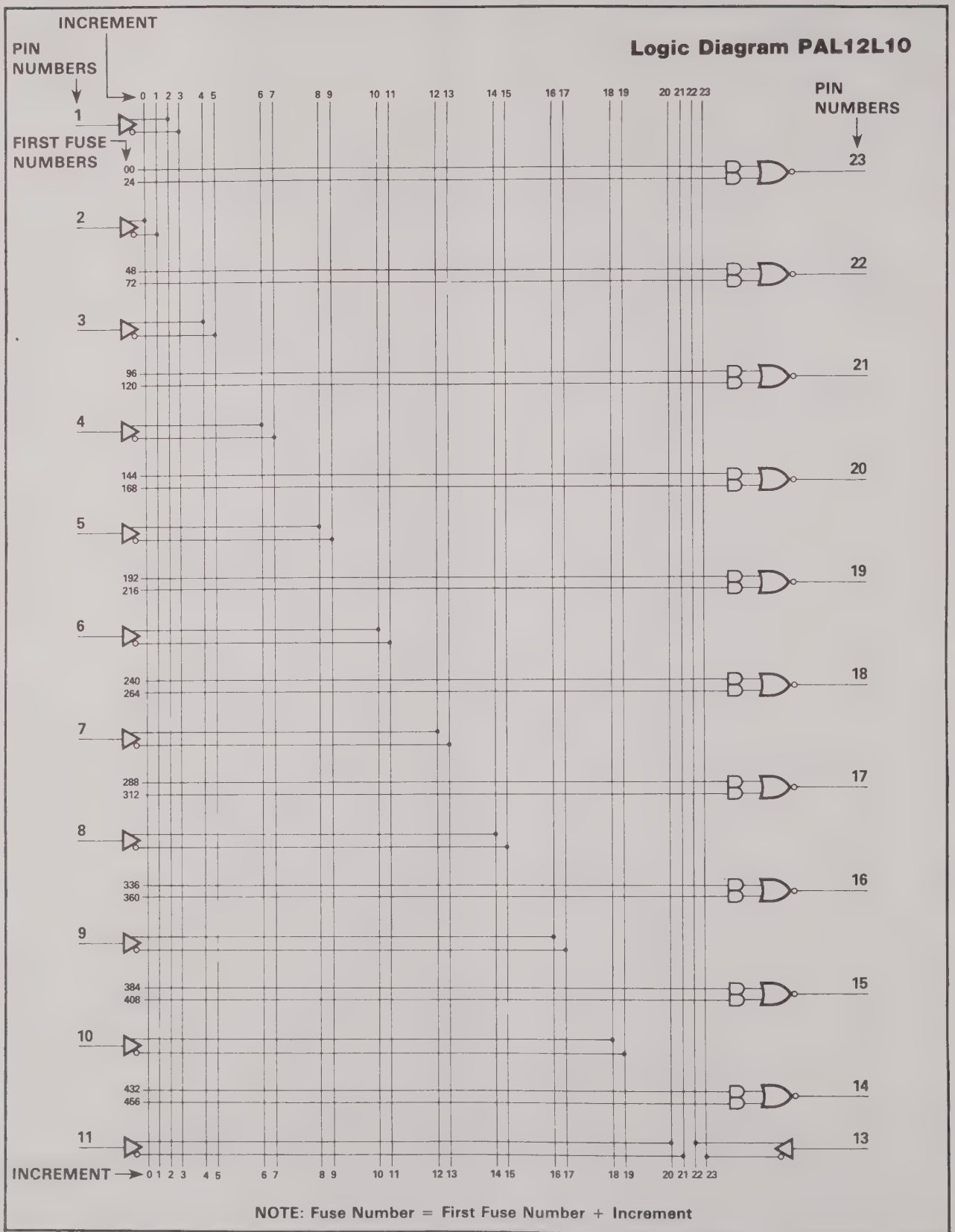


Figure A-7. Logic Diagram PAL12L10

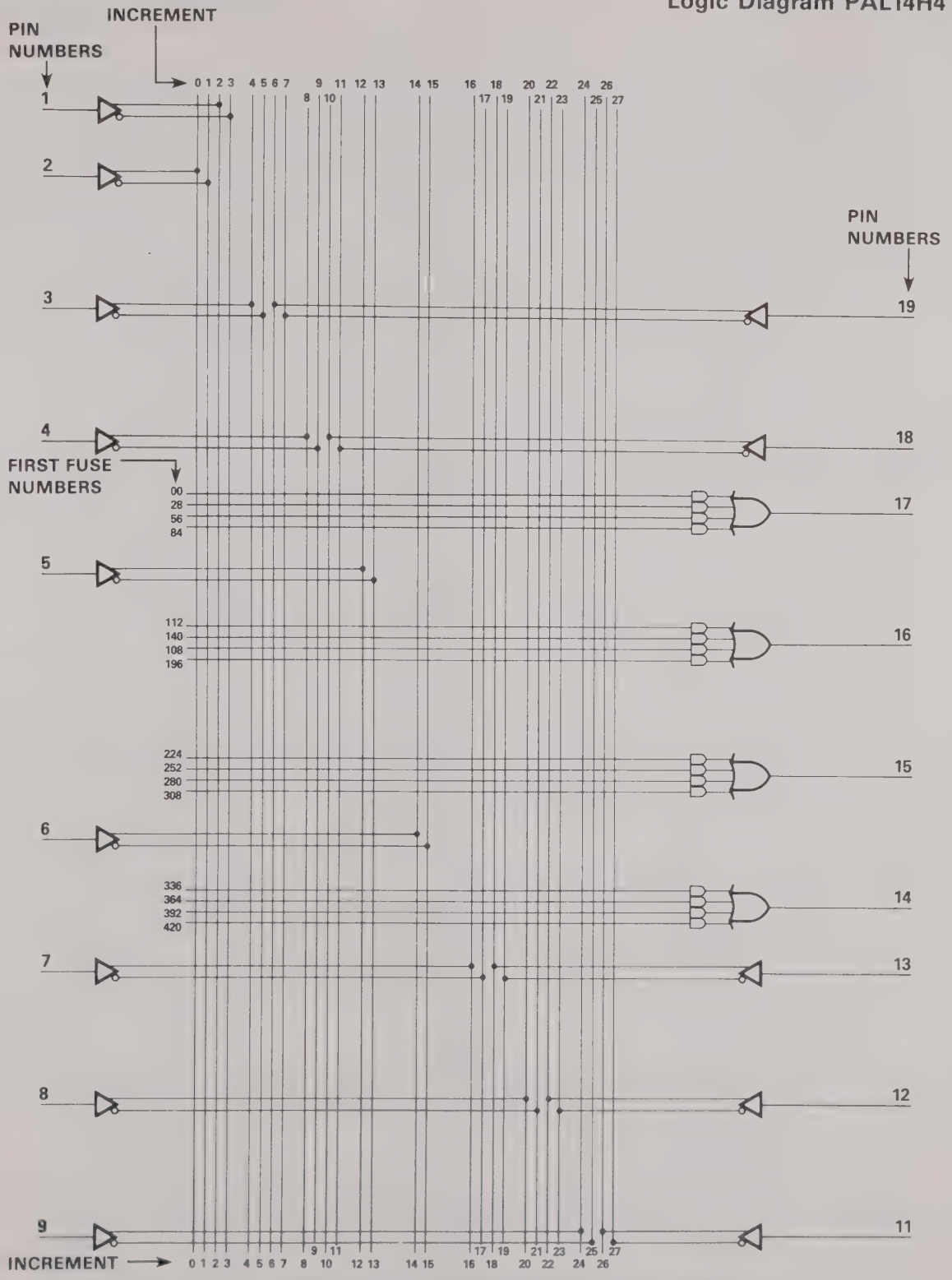
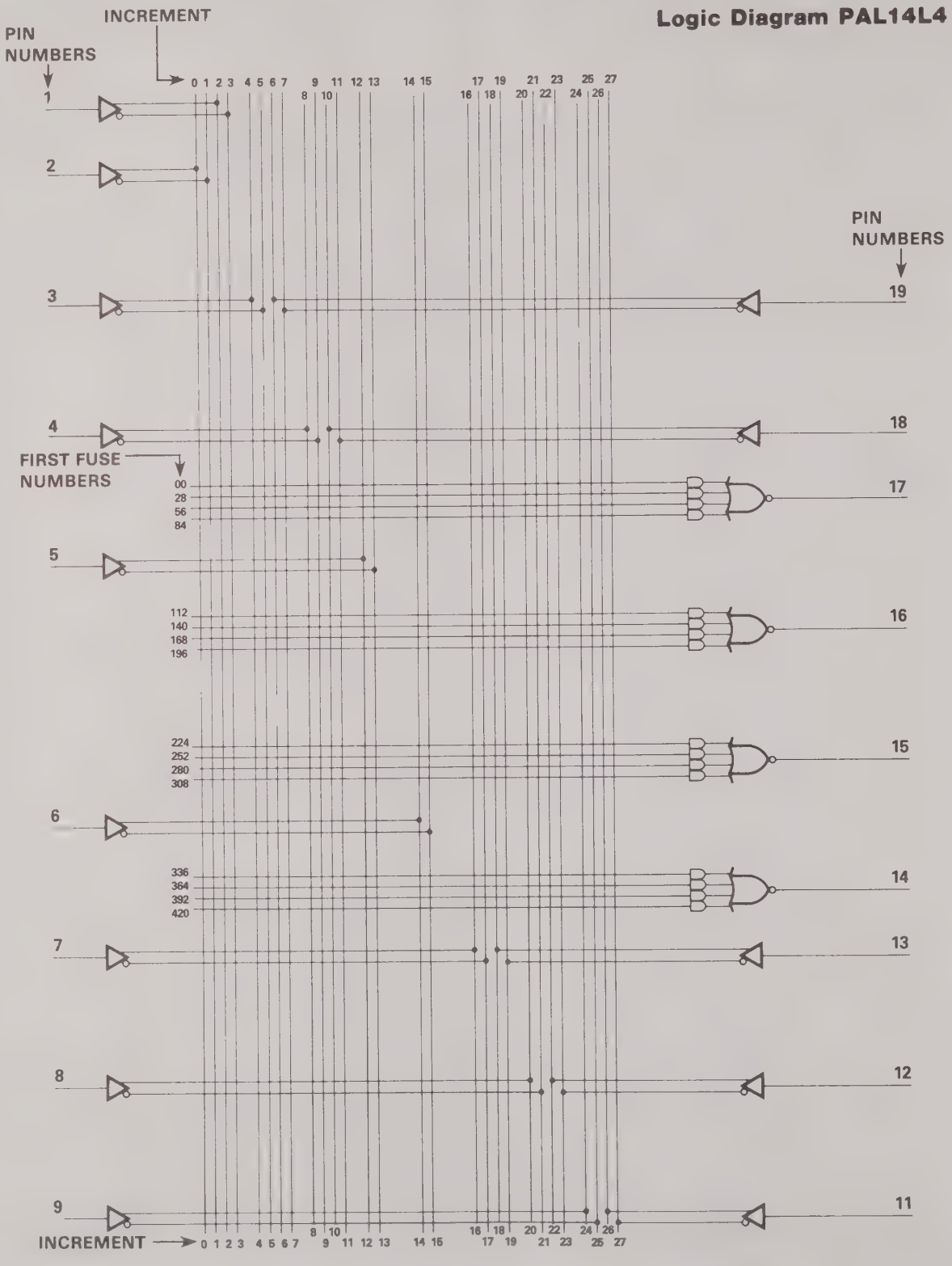


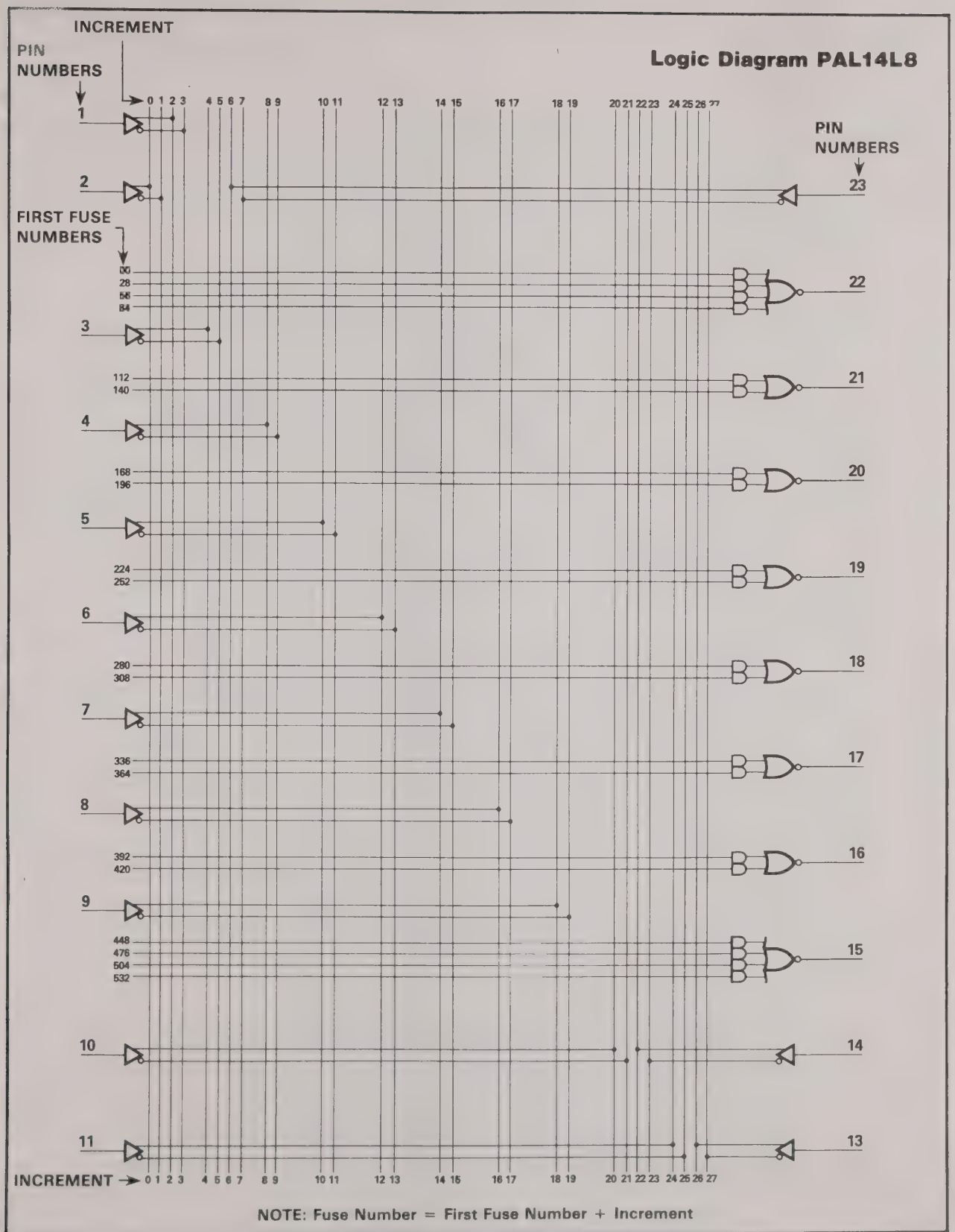
Figure A-8. Logic Diagram PAL14H4

Logic Diagram PAL14L4



NOTE: Fuse Number = First Fuse Number + Increment

Figure A-9. Logic Diagram PAL14L4



NOTE: Fuse Number = First Fuse Number + Increment

Figure A-10. Logic Diagram PAL14L8

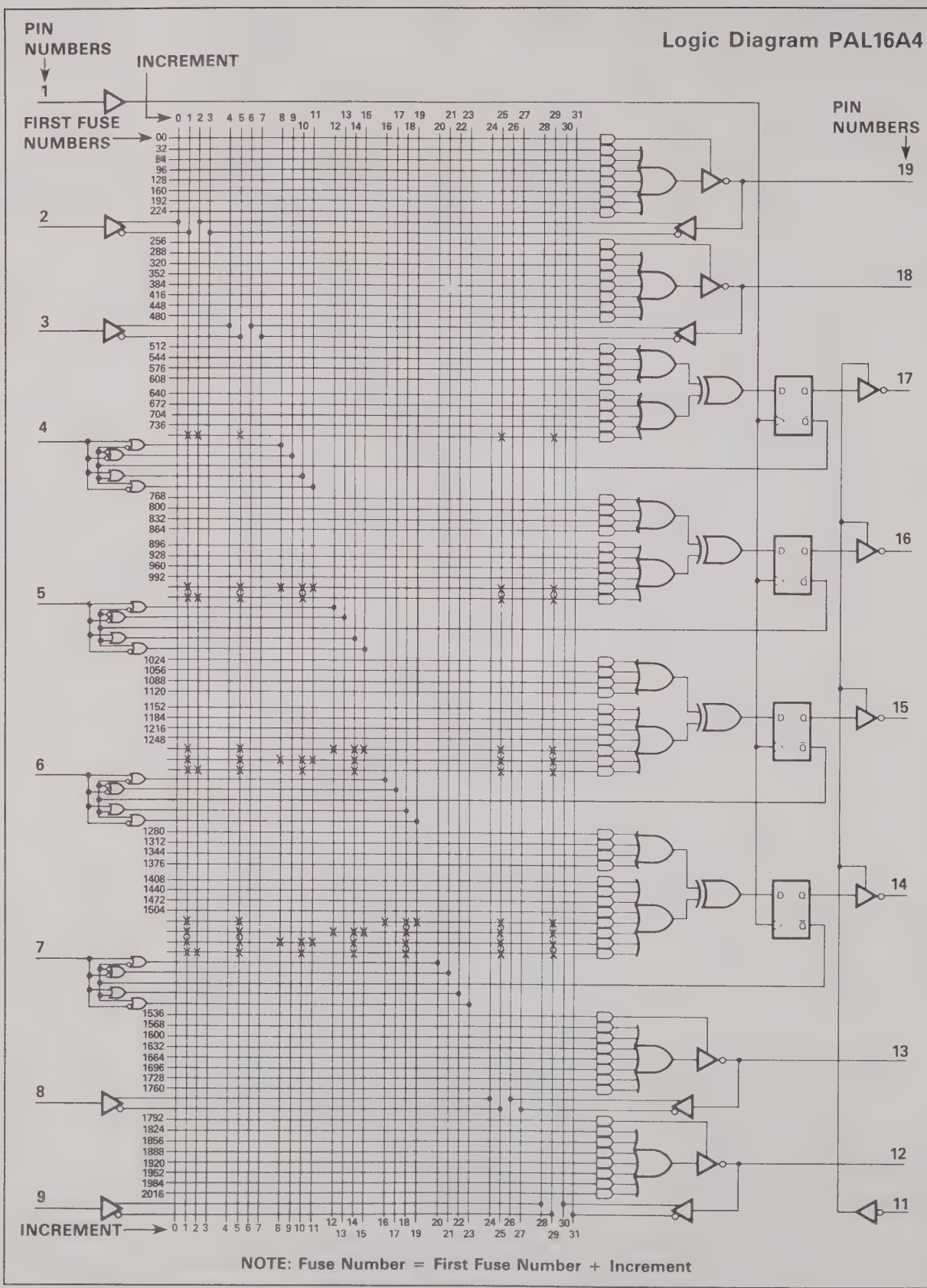


Figure A-11. Logic Diagram PAL16A4

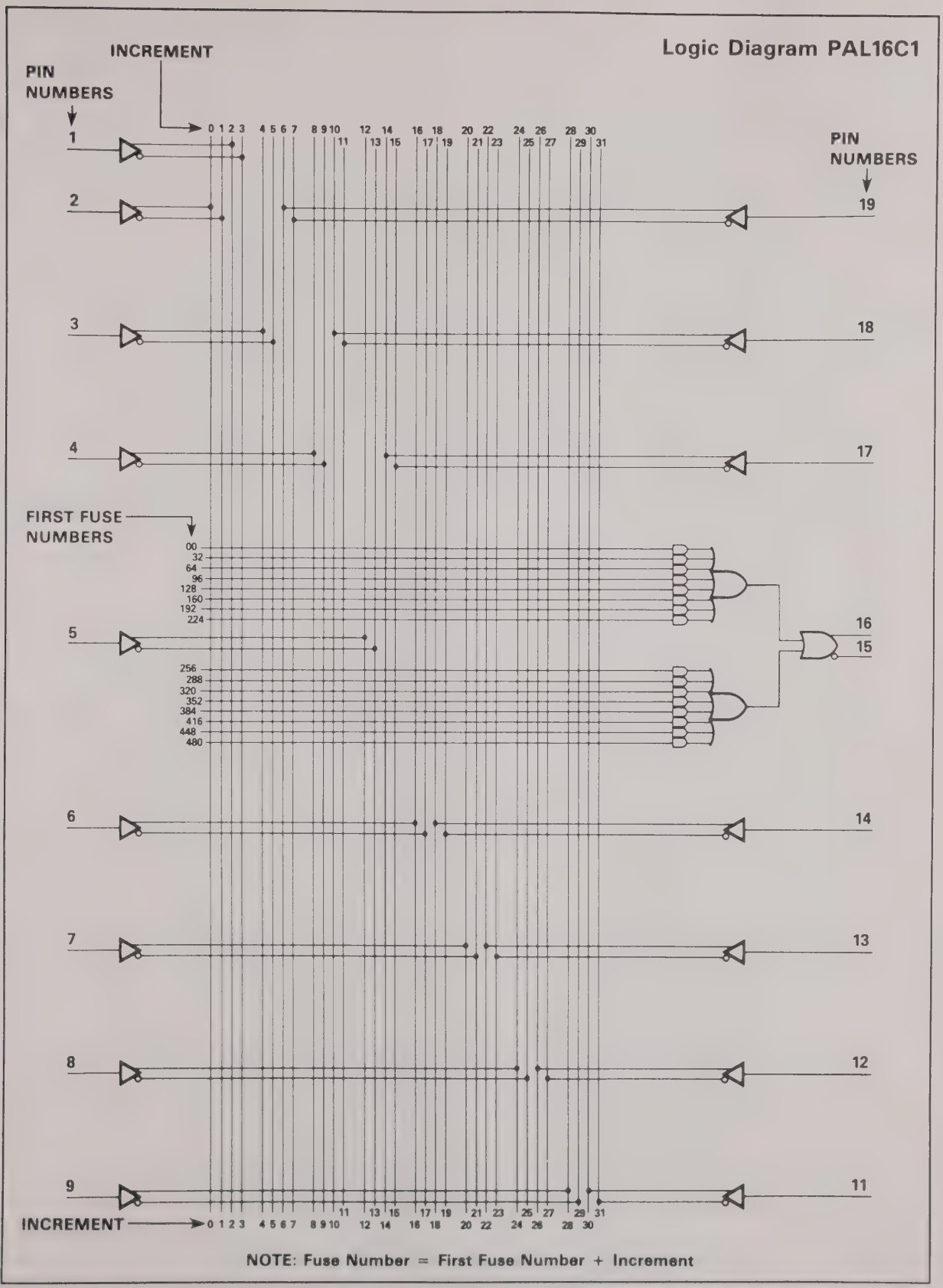
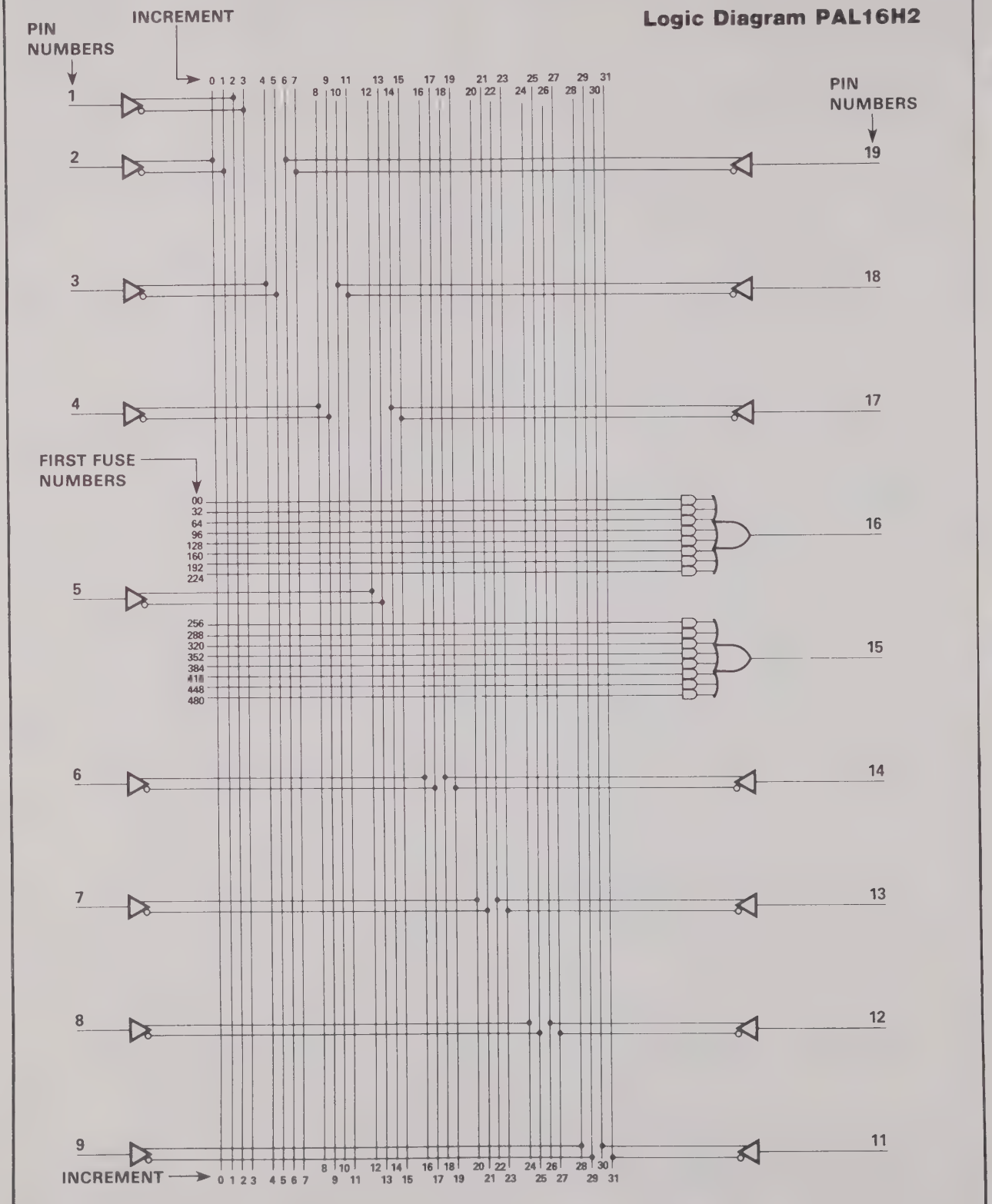


Figure A-12. Logic Diagram PAL16C1



NOTE: Fuse Number = First Fuse Number + Increment

Figure A-13. Logic Diagram PAL16H2

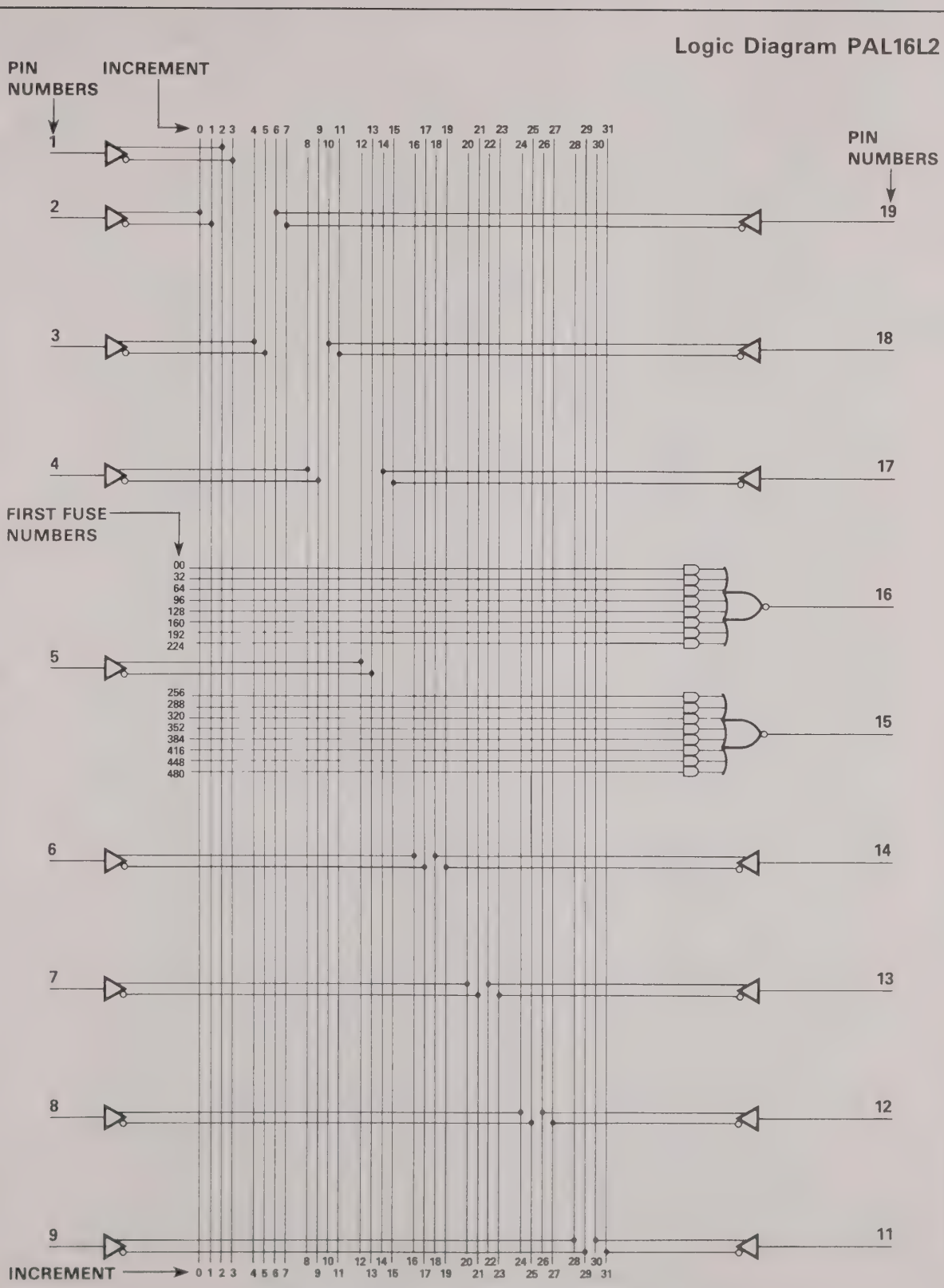


Figure A-14. Logic Diagram PAL16L2

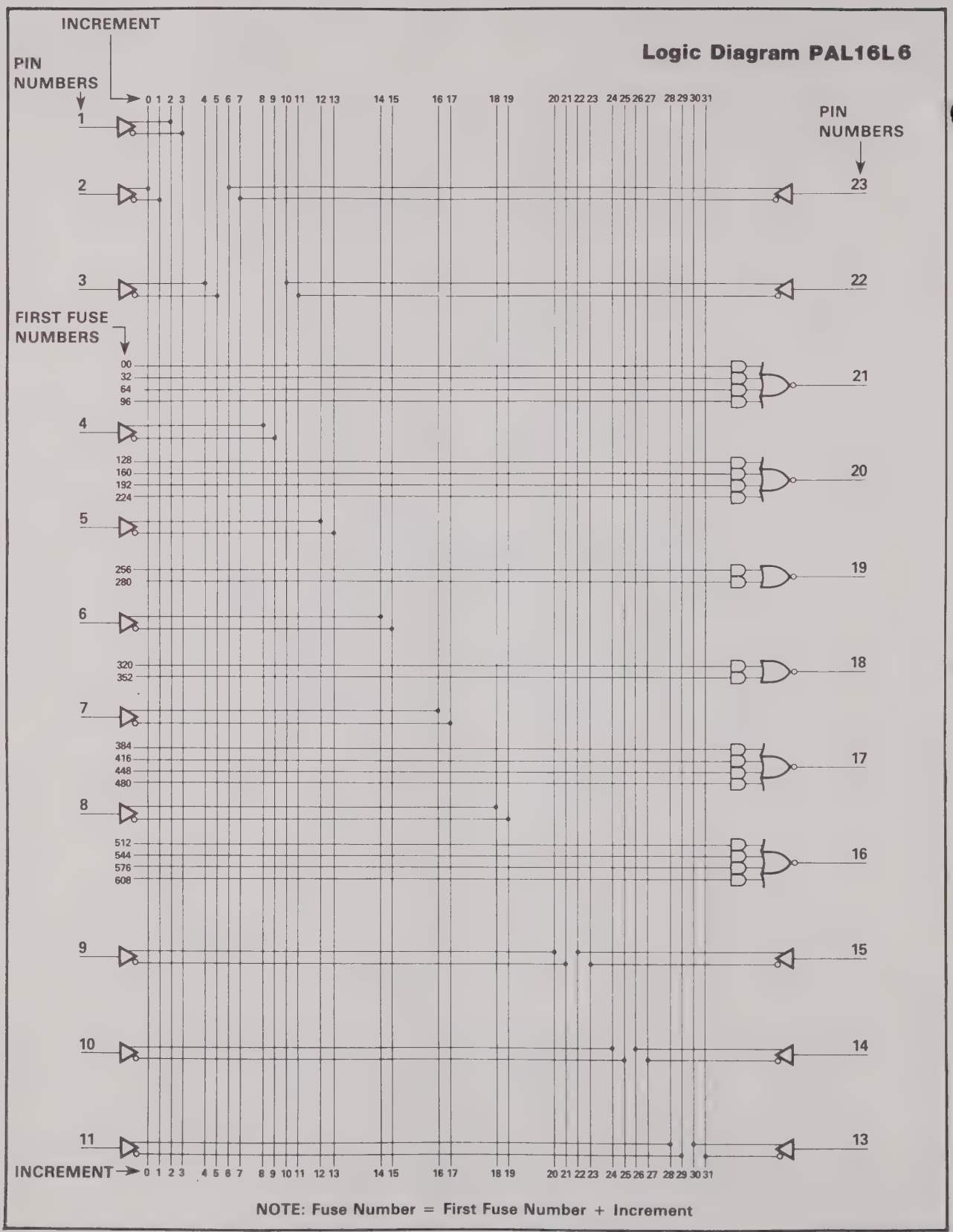
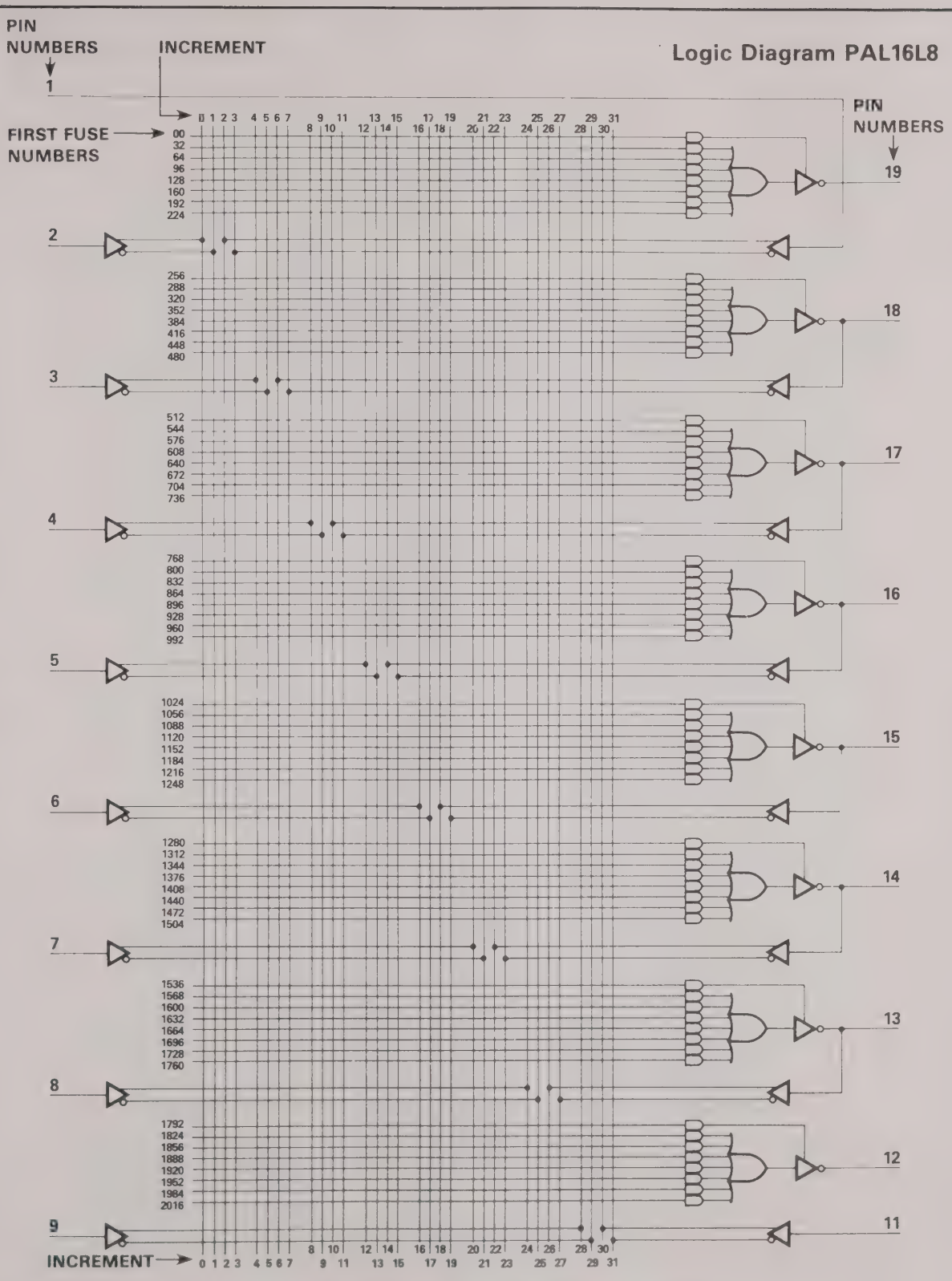
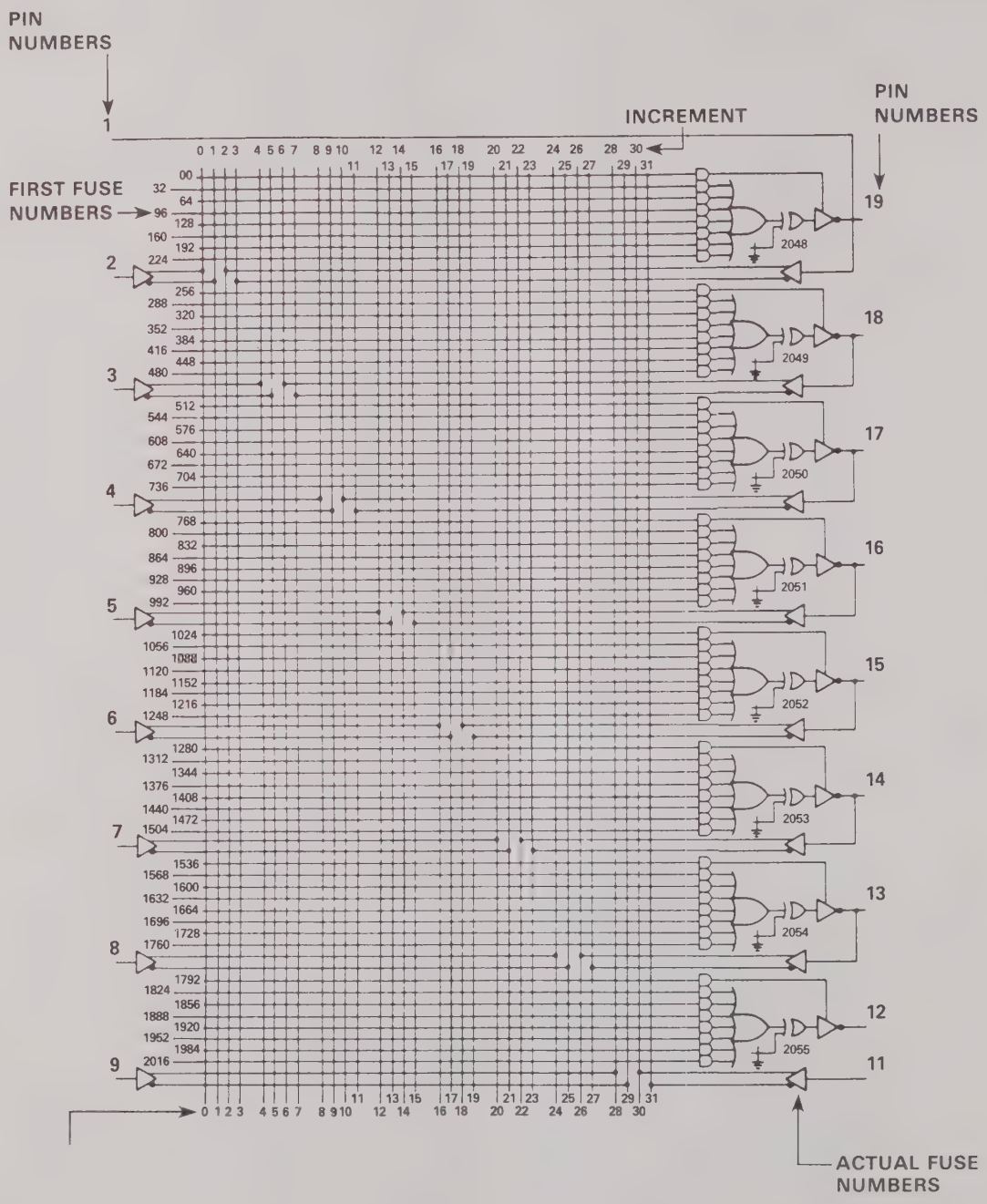


Figure A-15. Logic Diagram PAL16L6



NOTE: Fuse Number = First Fuse Number + Increment

Figure A-16. Logic Diagram PAL16L8



NOTE: Fuse Number = First Fuse Number + Increment

Figure A-17. Logic Diagram PAL16P8

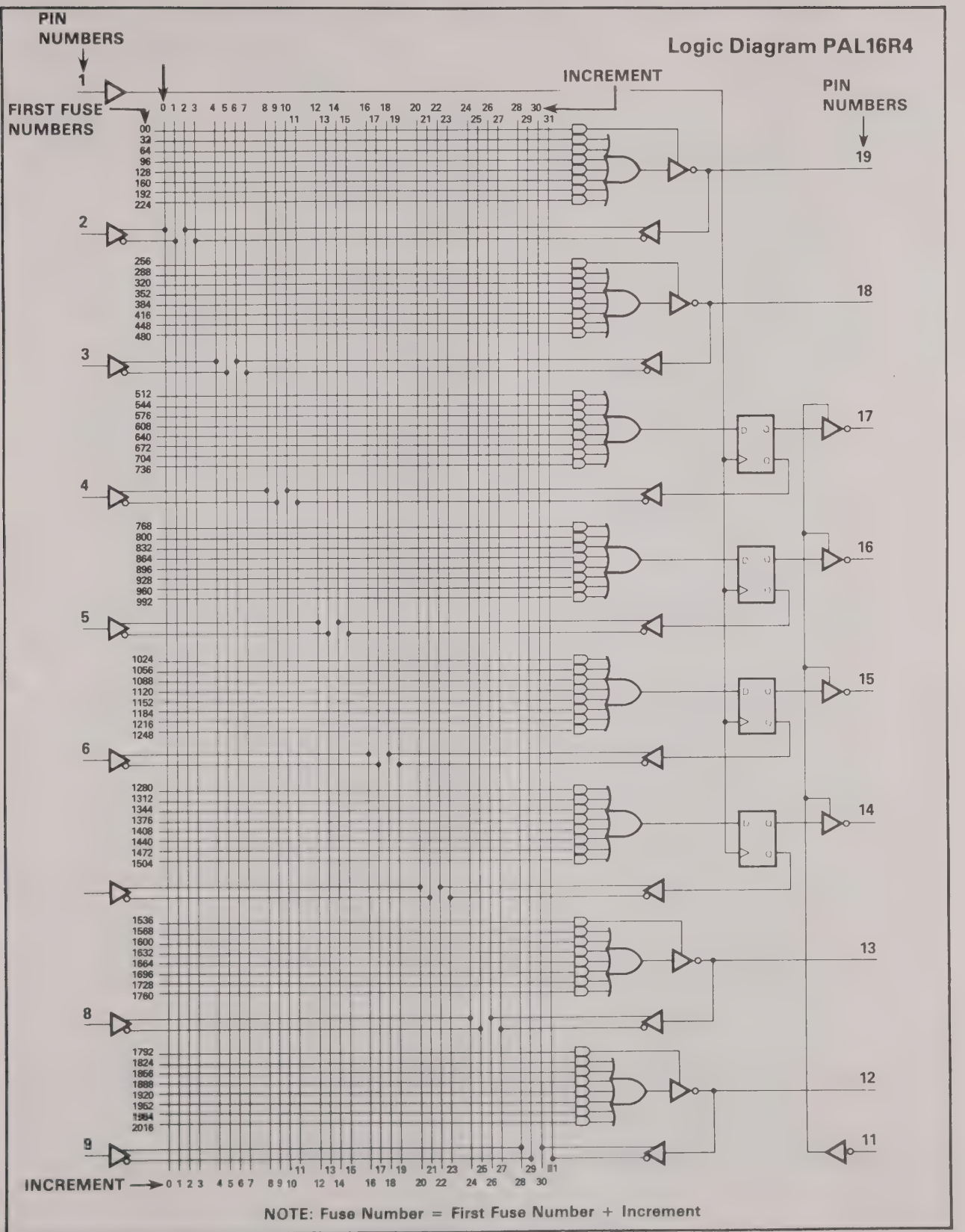


Figure A-18. Logic Diagram PAL16R4

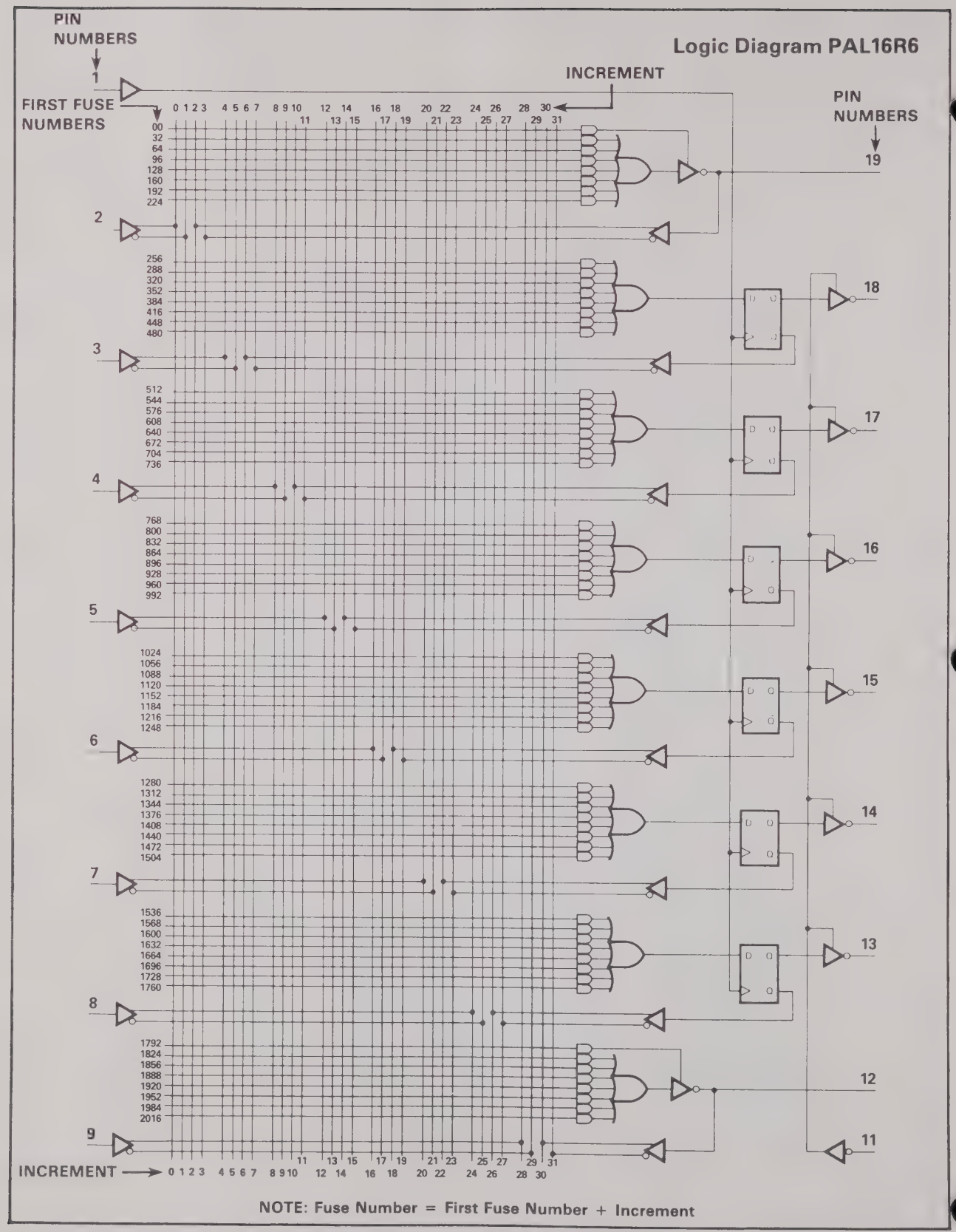


Figure A-19. Logic Diagram PAL16R6

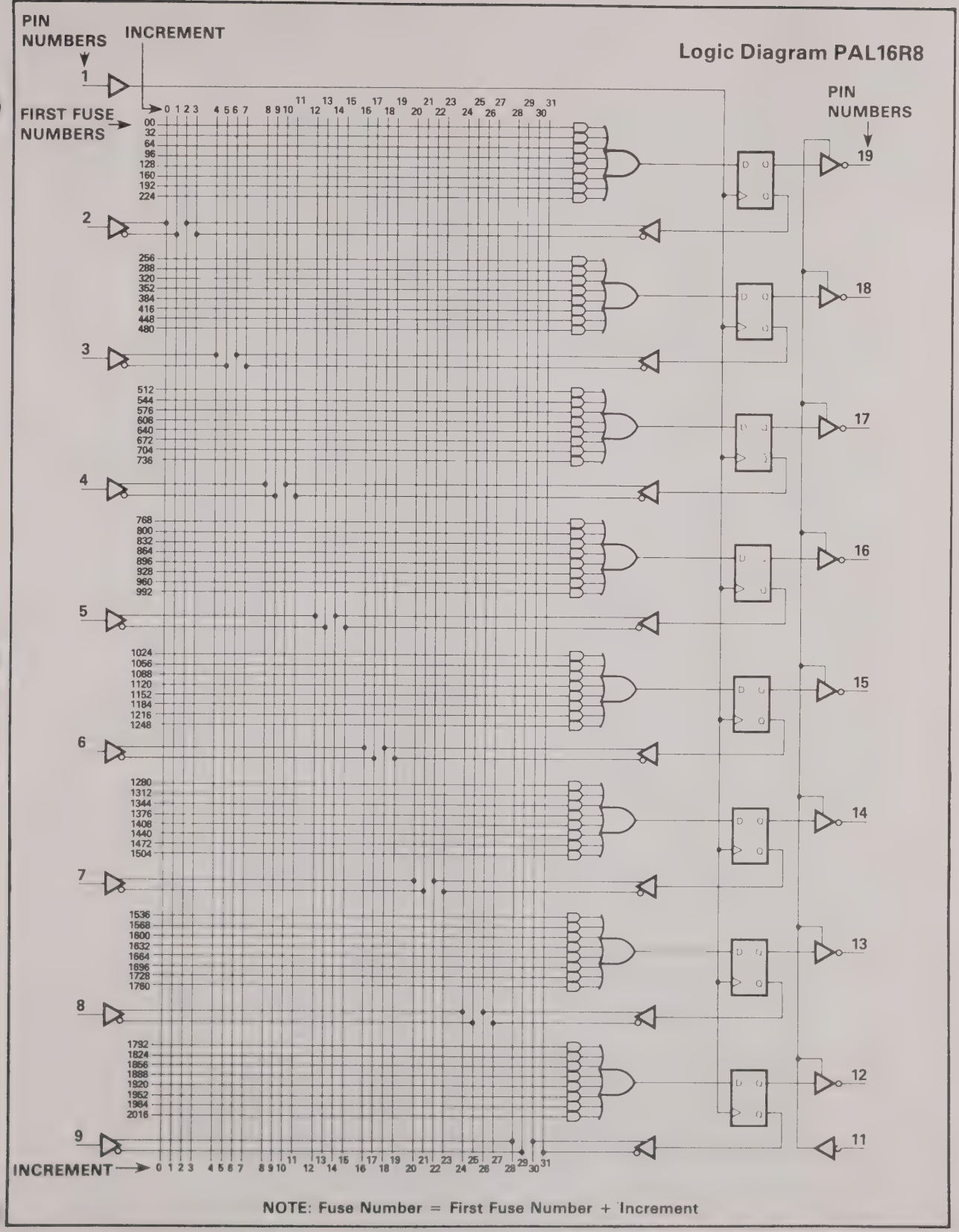


Figure A-20. Logic Diagram PAL16R8

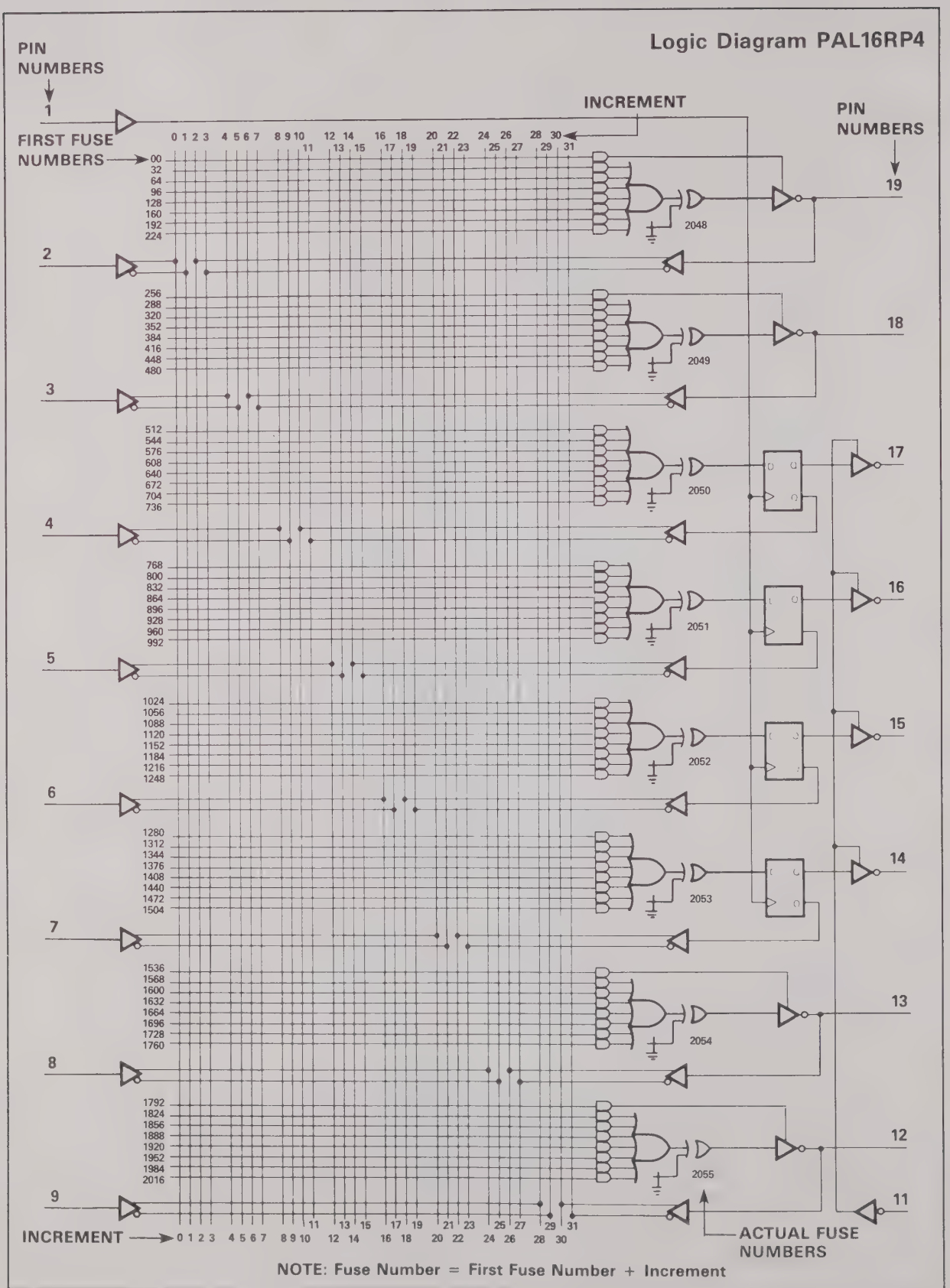


Figure A-21. Logic Diagram PAL16RP4

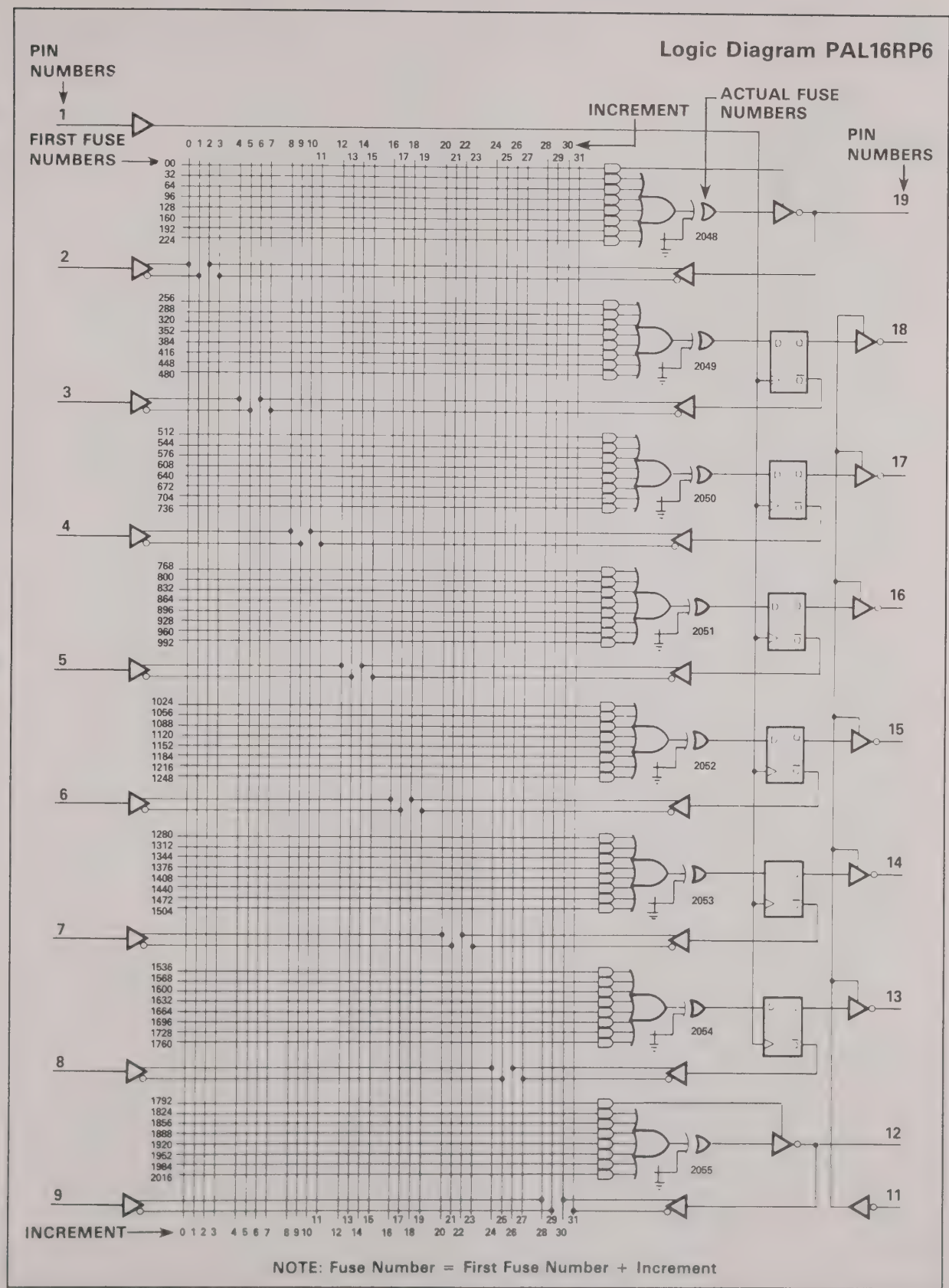


Figure A-22. Logic Diagram PAL16RP6

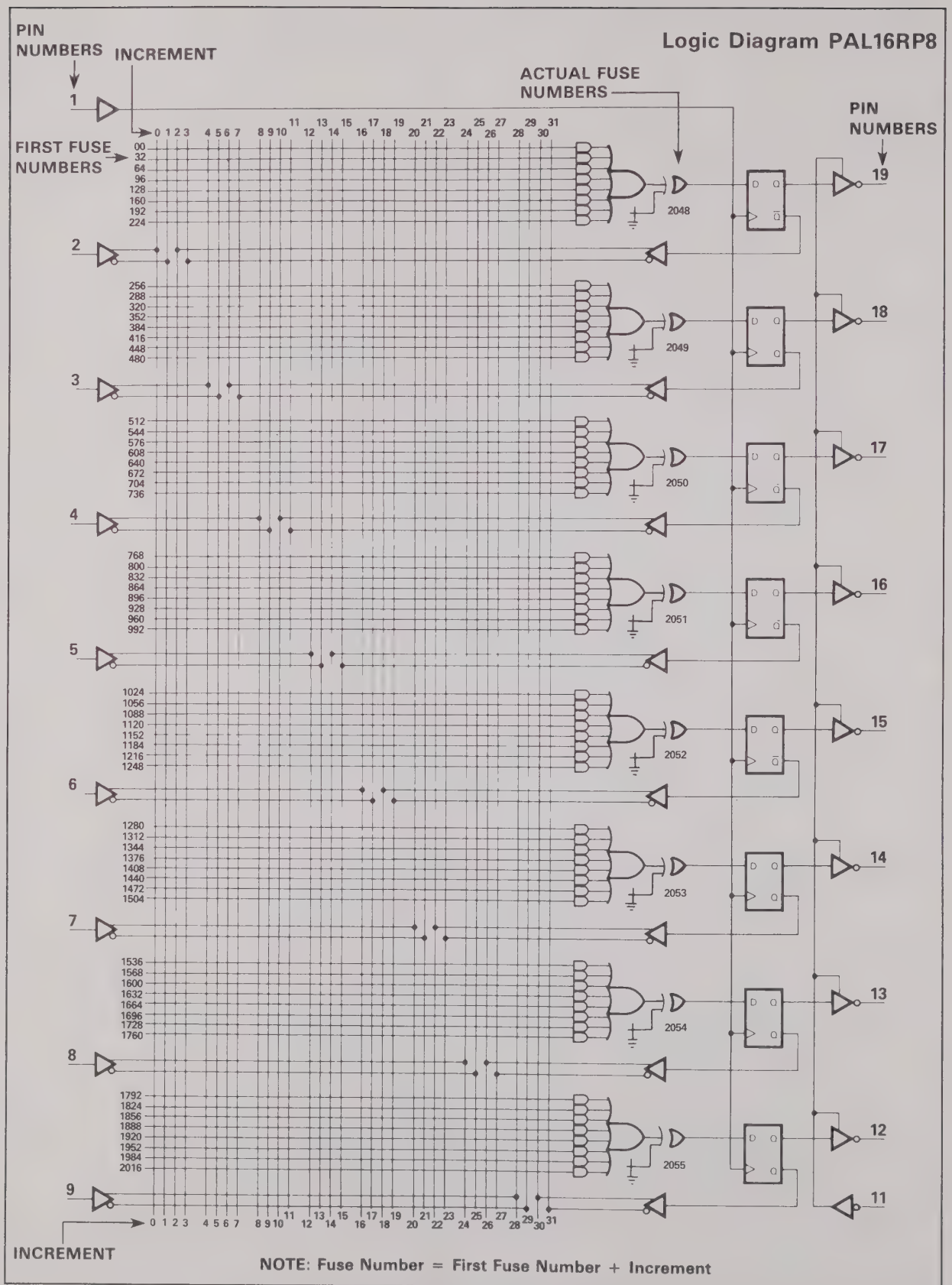


Figure A-23. Logic Diagram PAL16RP8

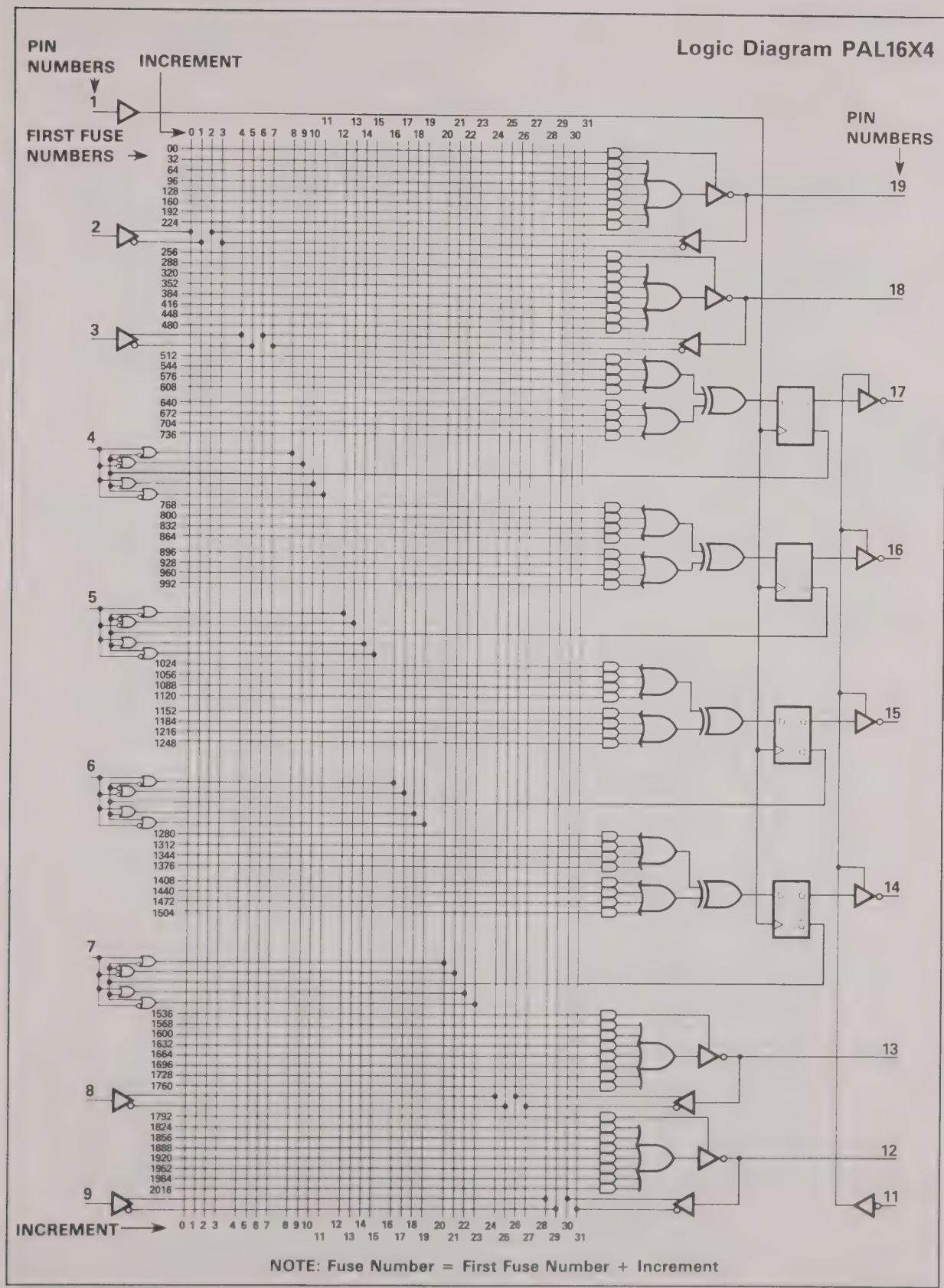


Figure A-24. Logic Diagram PAL16X4

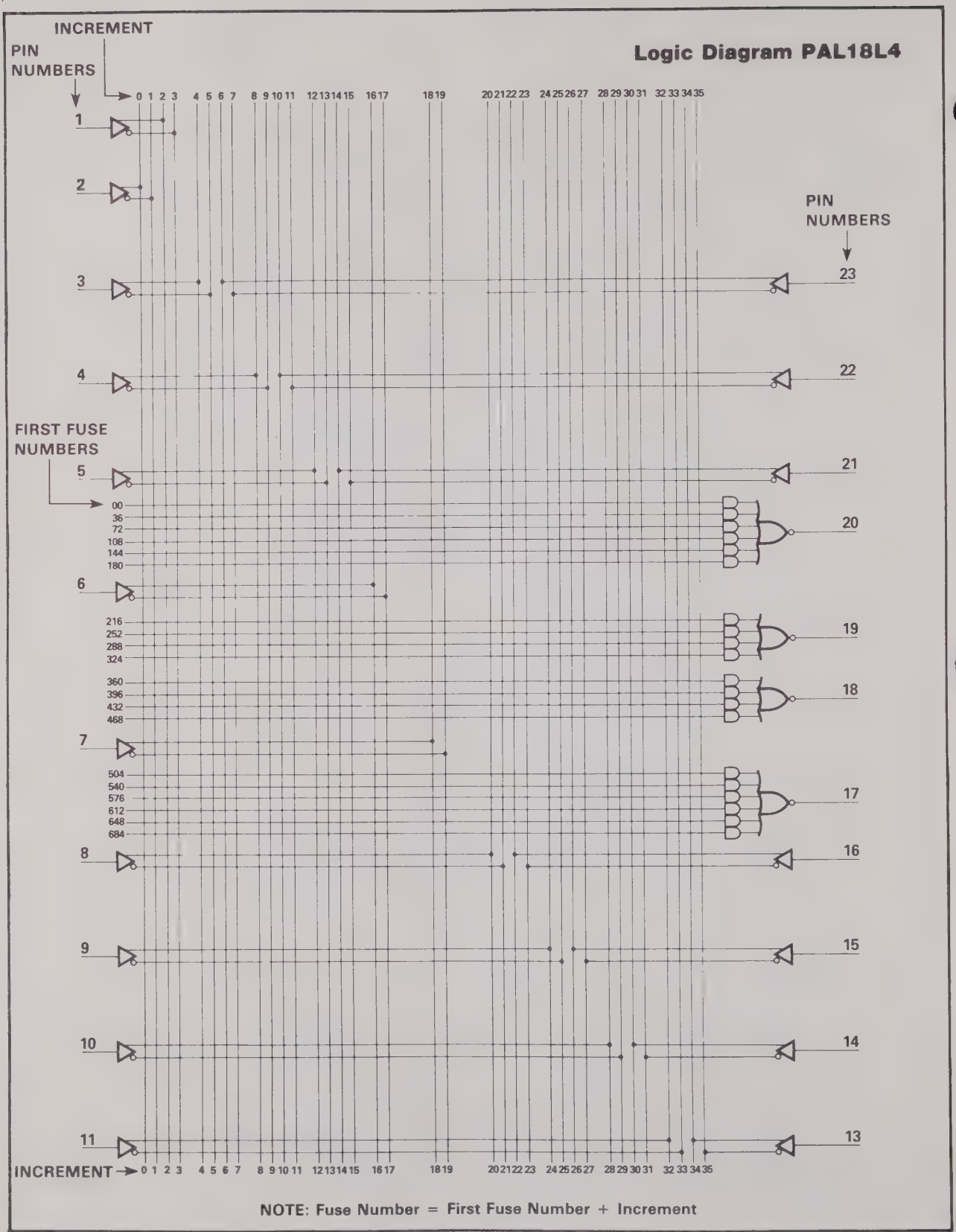


Figure A-25. Logic Diagram PAL18L4

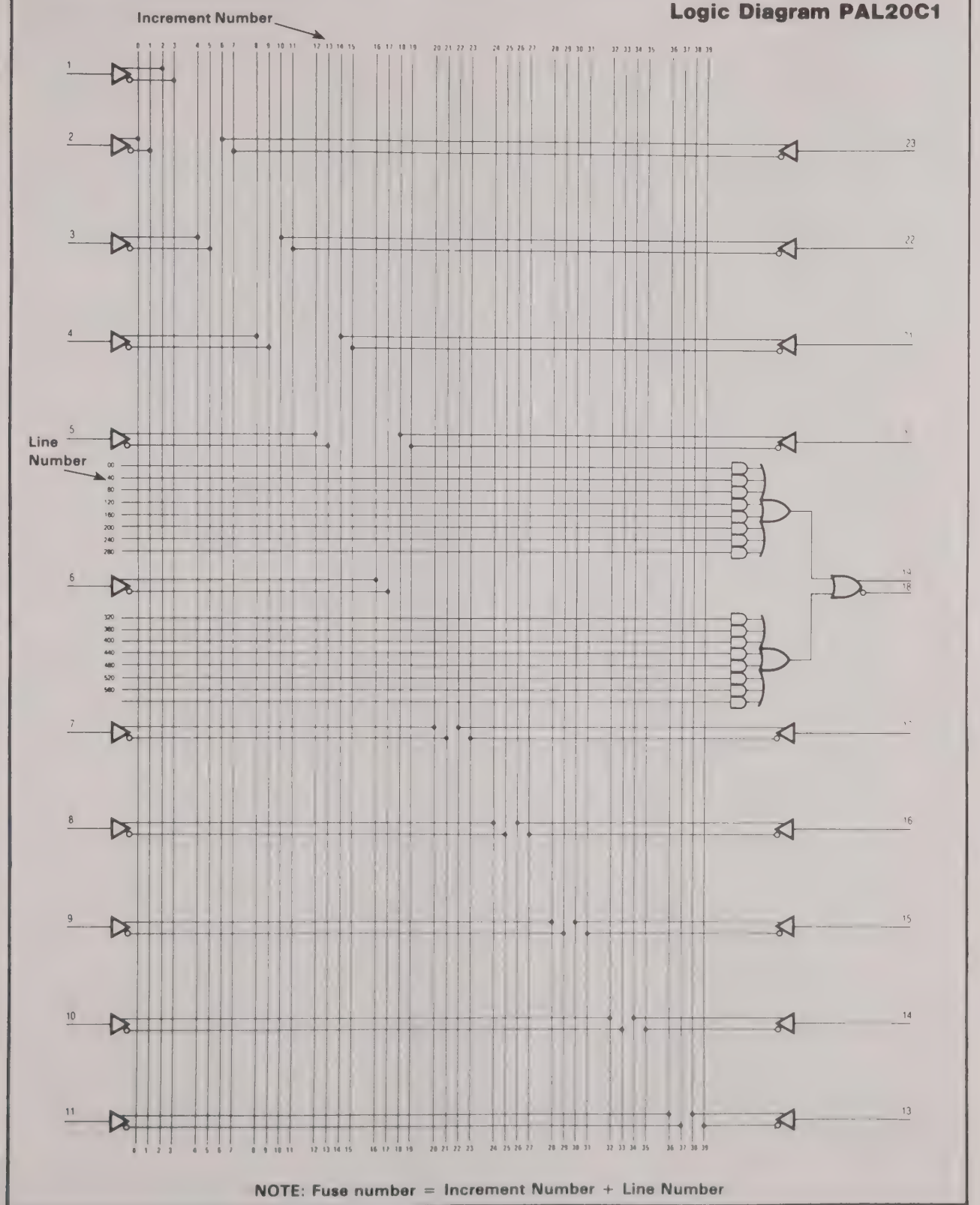
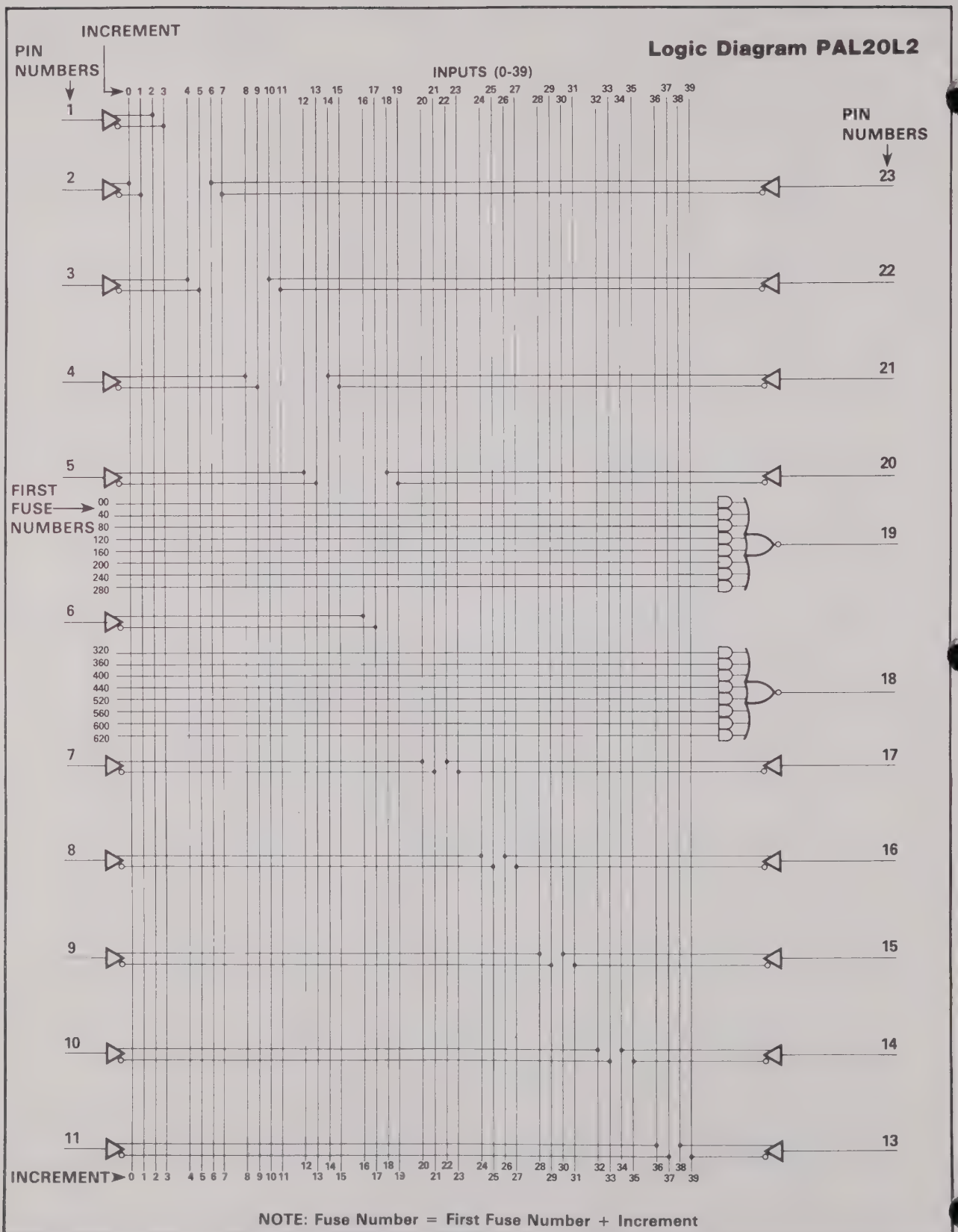


Figure A-26. Logic Diagram PAL20C1



NOTE: Fuse Number = First Fuse Number + Increment

Figure A-27. Logic Diagram PAL20L2

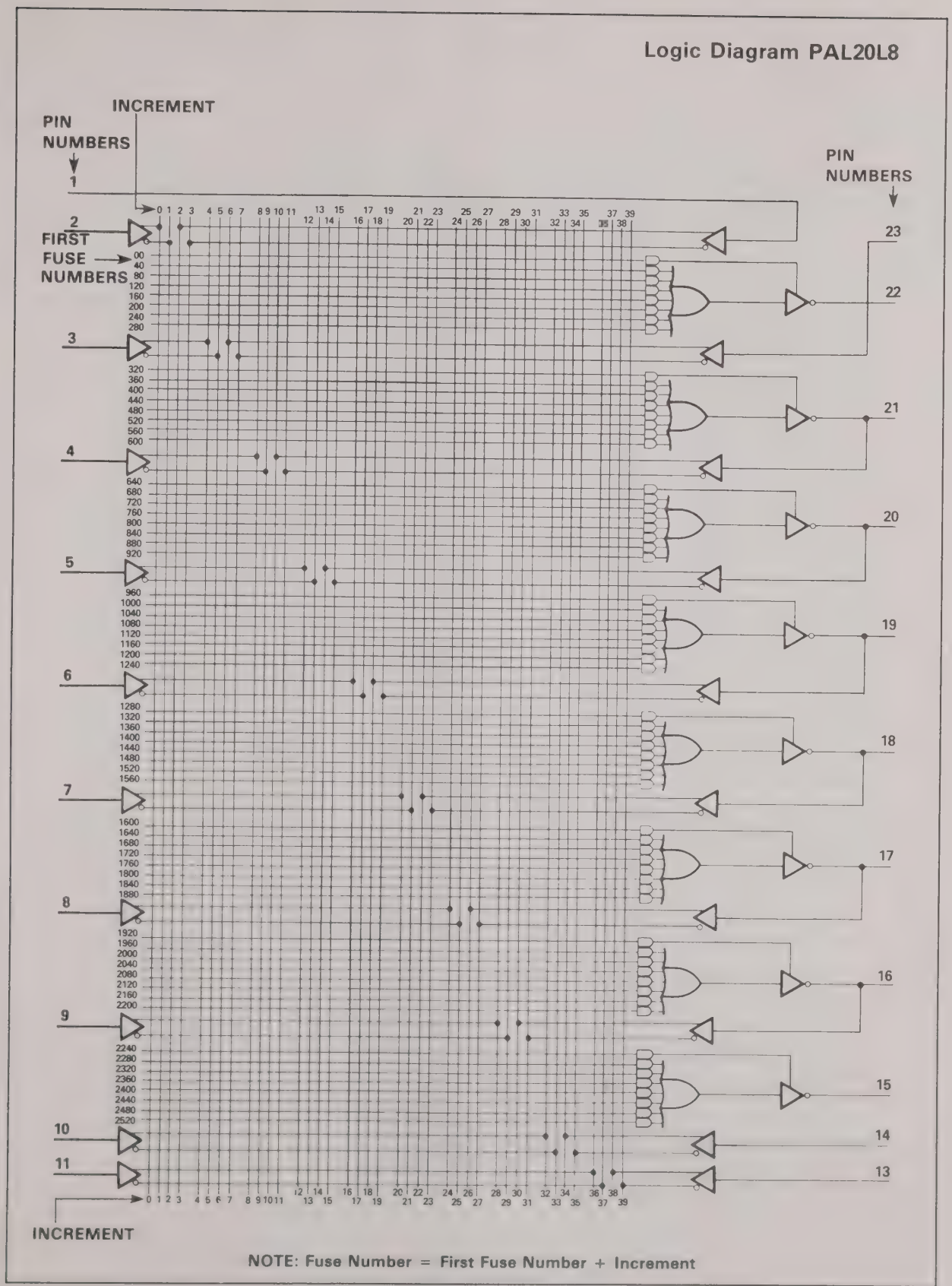


Figure A-28. Logic Diagram PAL20L8

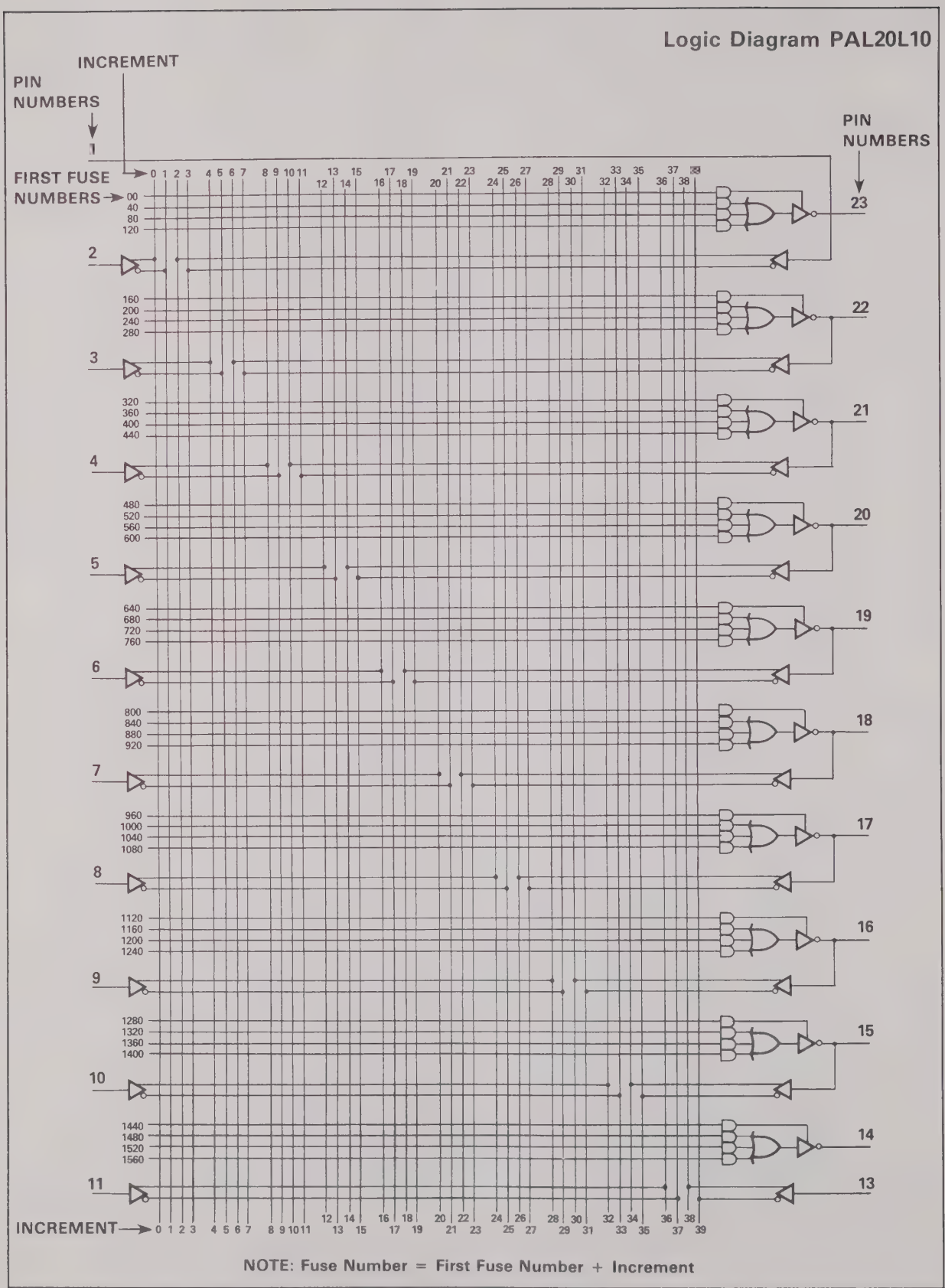


Figure A-29. Logic Diagram PAL20L10

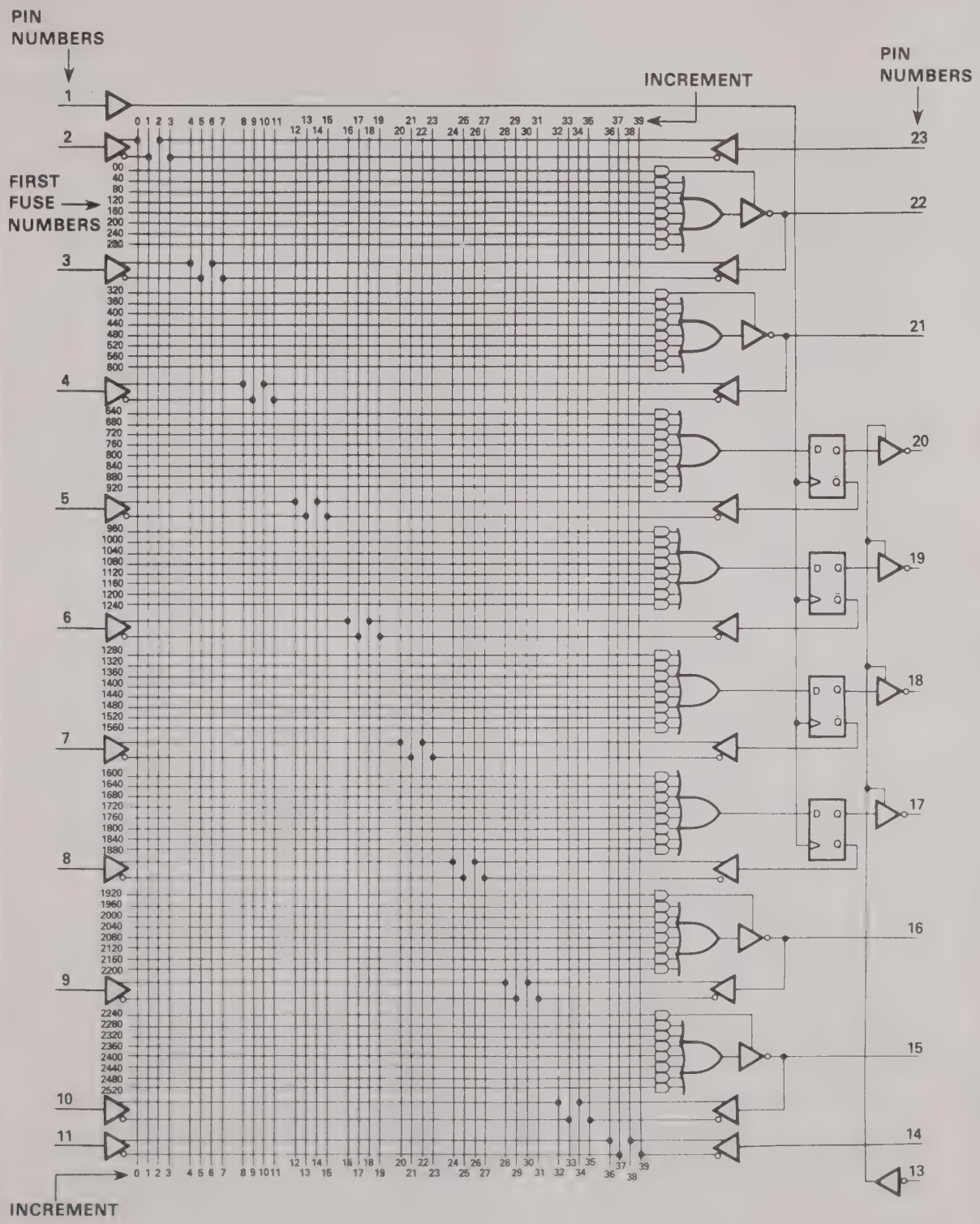


Figure A-30. Logic Diagram PAL20R4

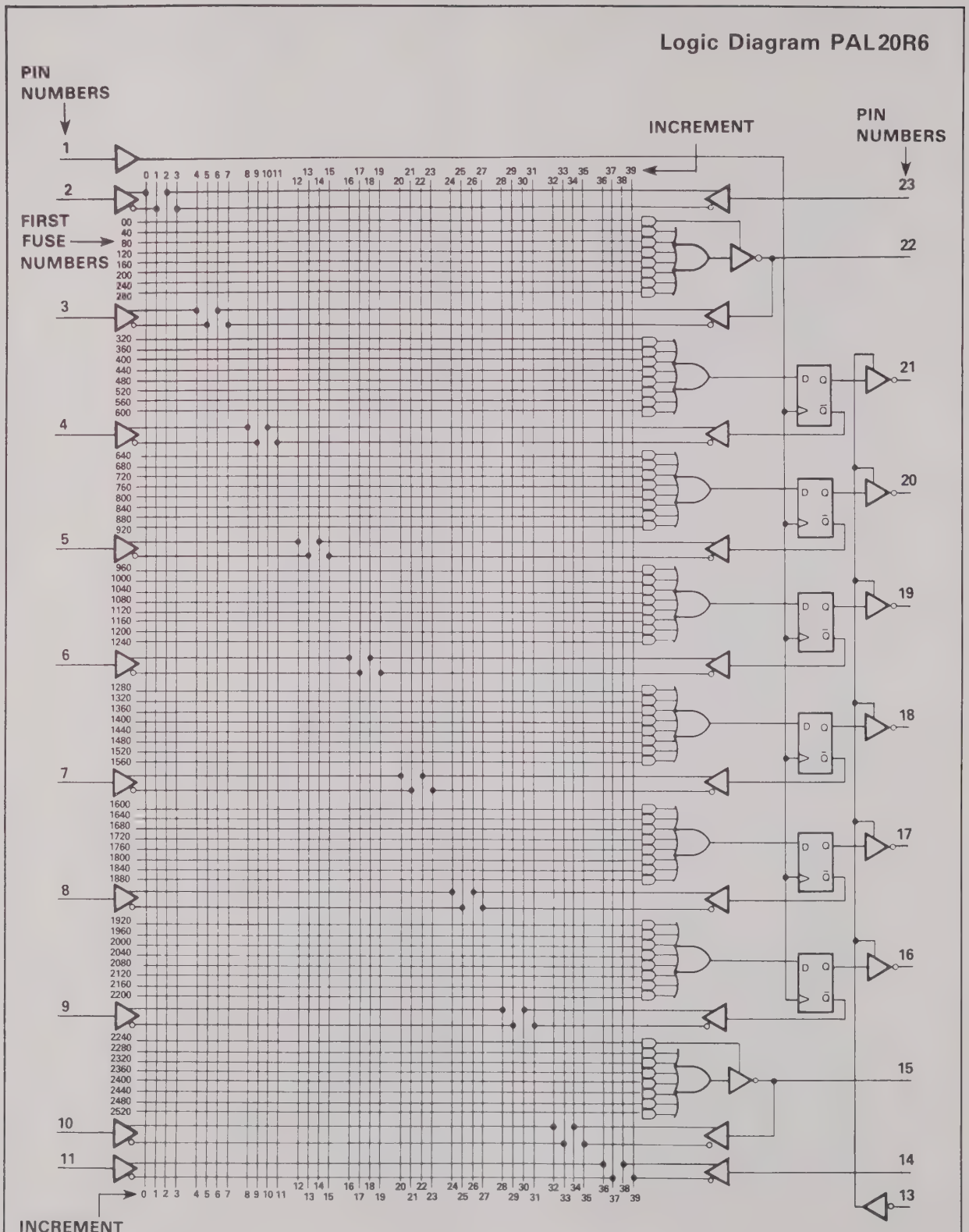


Figure A-31. Logic Diagram PAL20R6

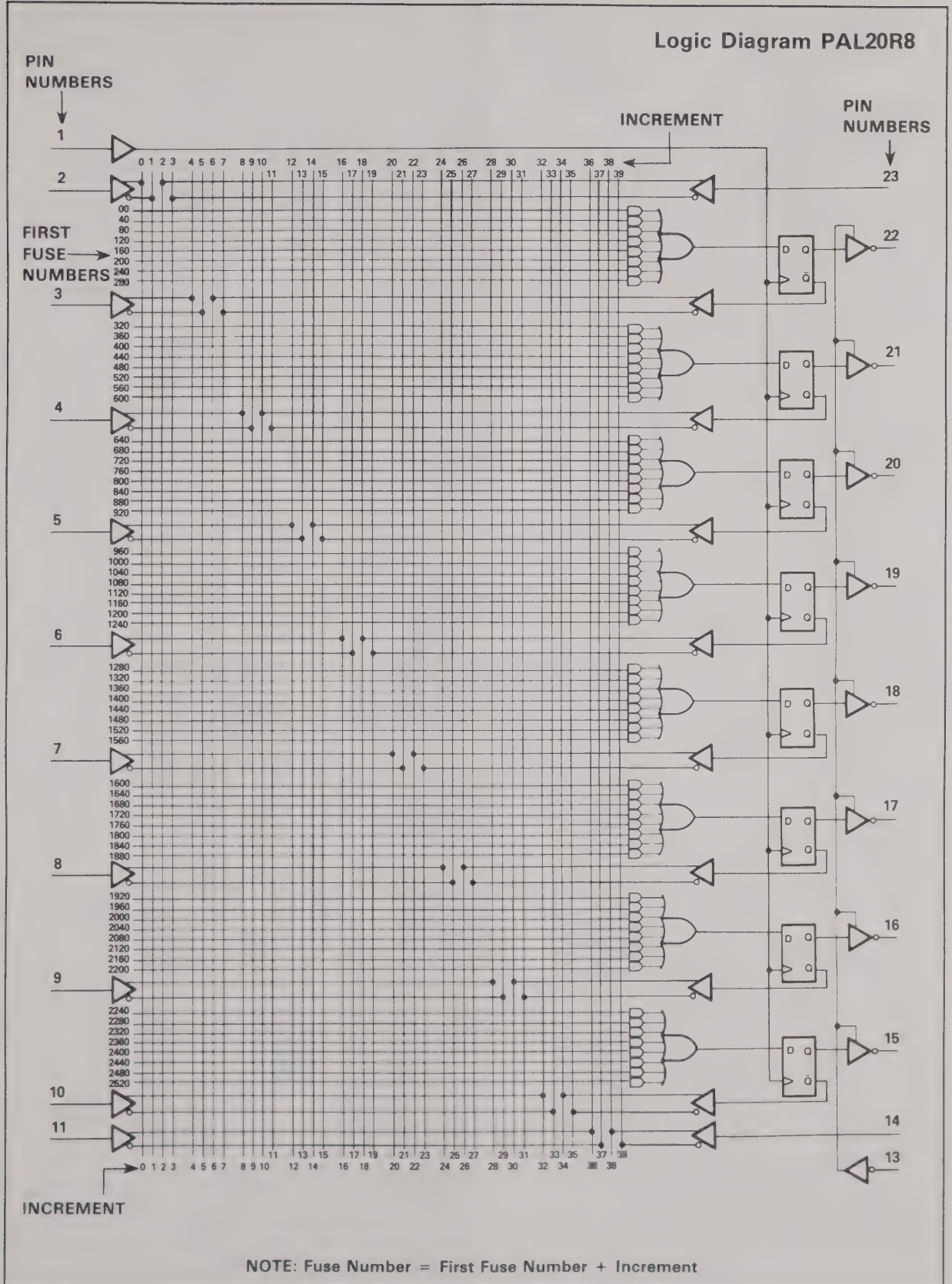
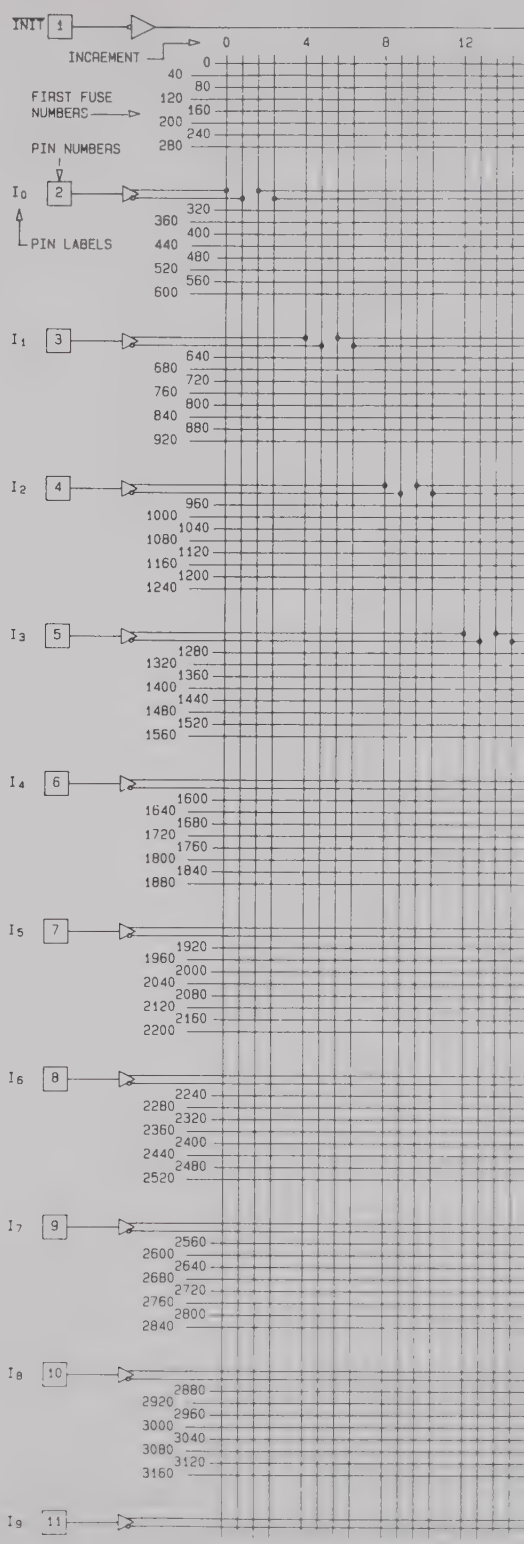
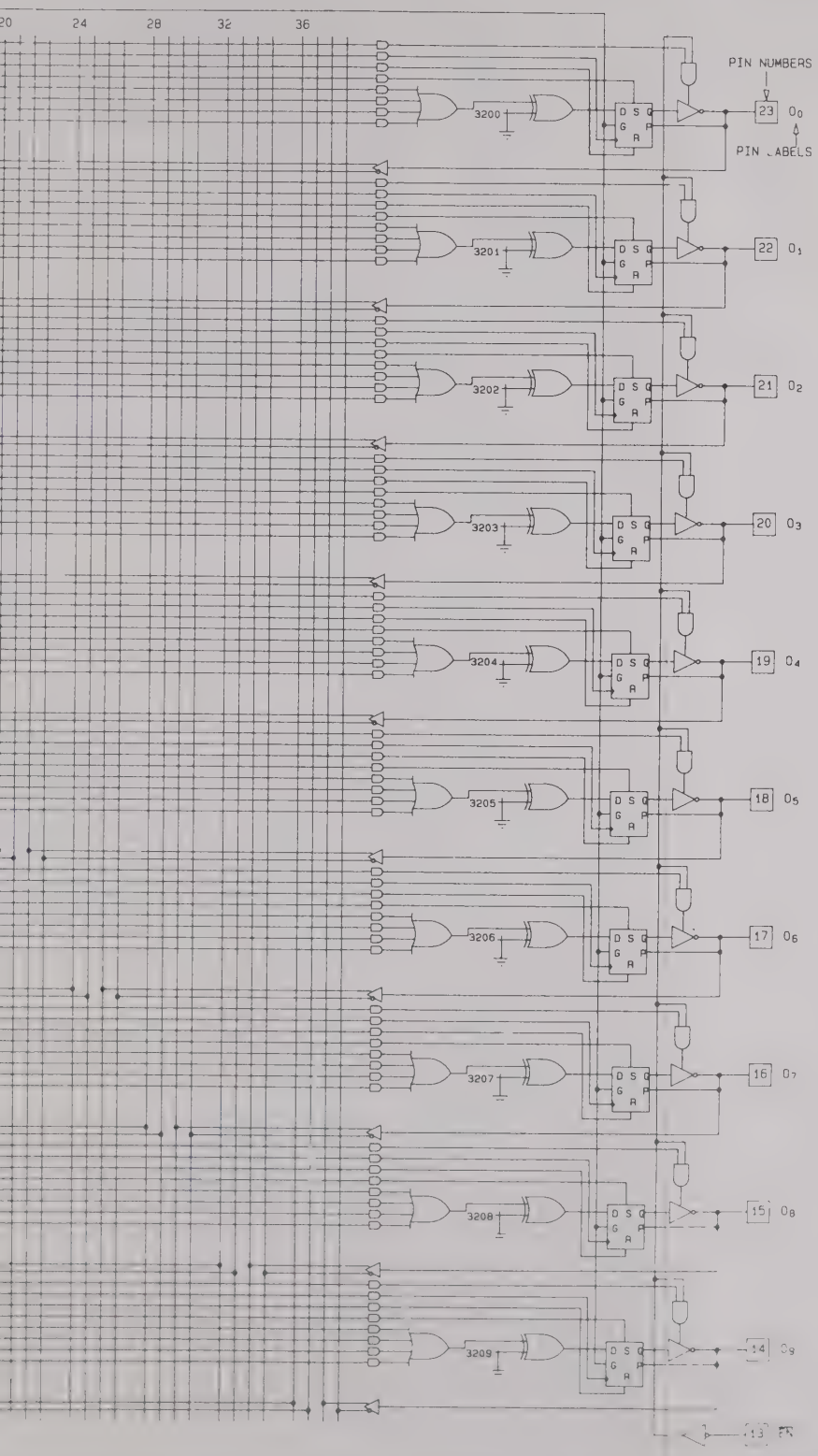


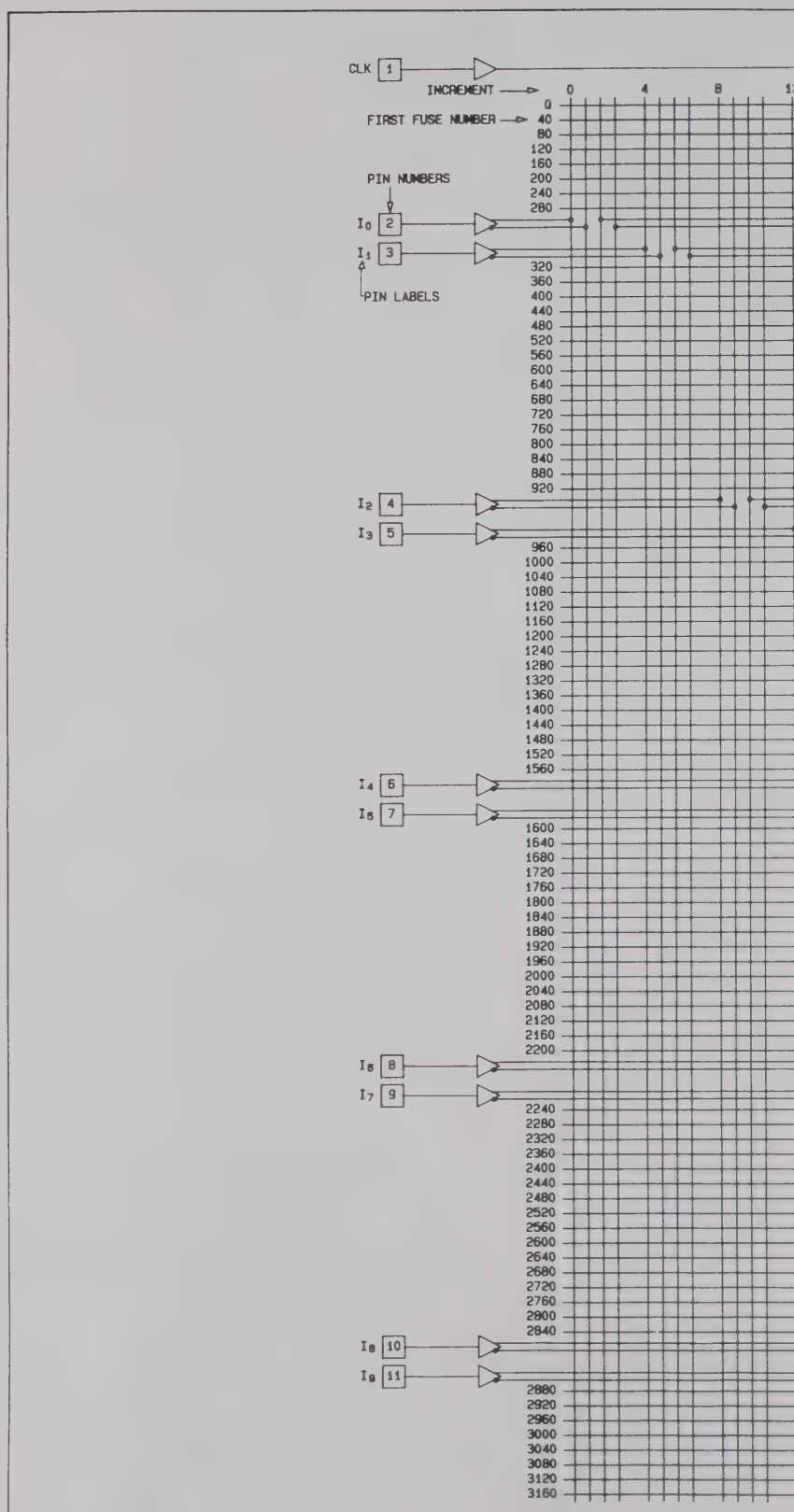
Figure A-32. Logic Diagram PAL20R8



NOTE: FUSE NUMBER = FIRST FUSE NUMBER



A-33. Logic Diagram PAL20RA10



NOTE: FUSE NUMBER = FIRST FUSE NUMBER + INCREMENT

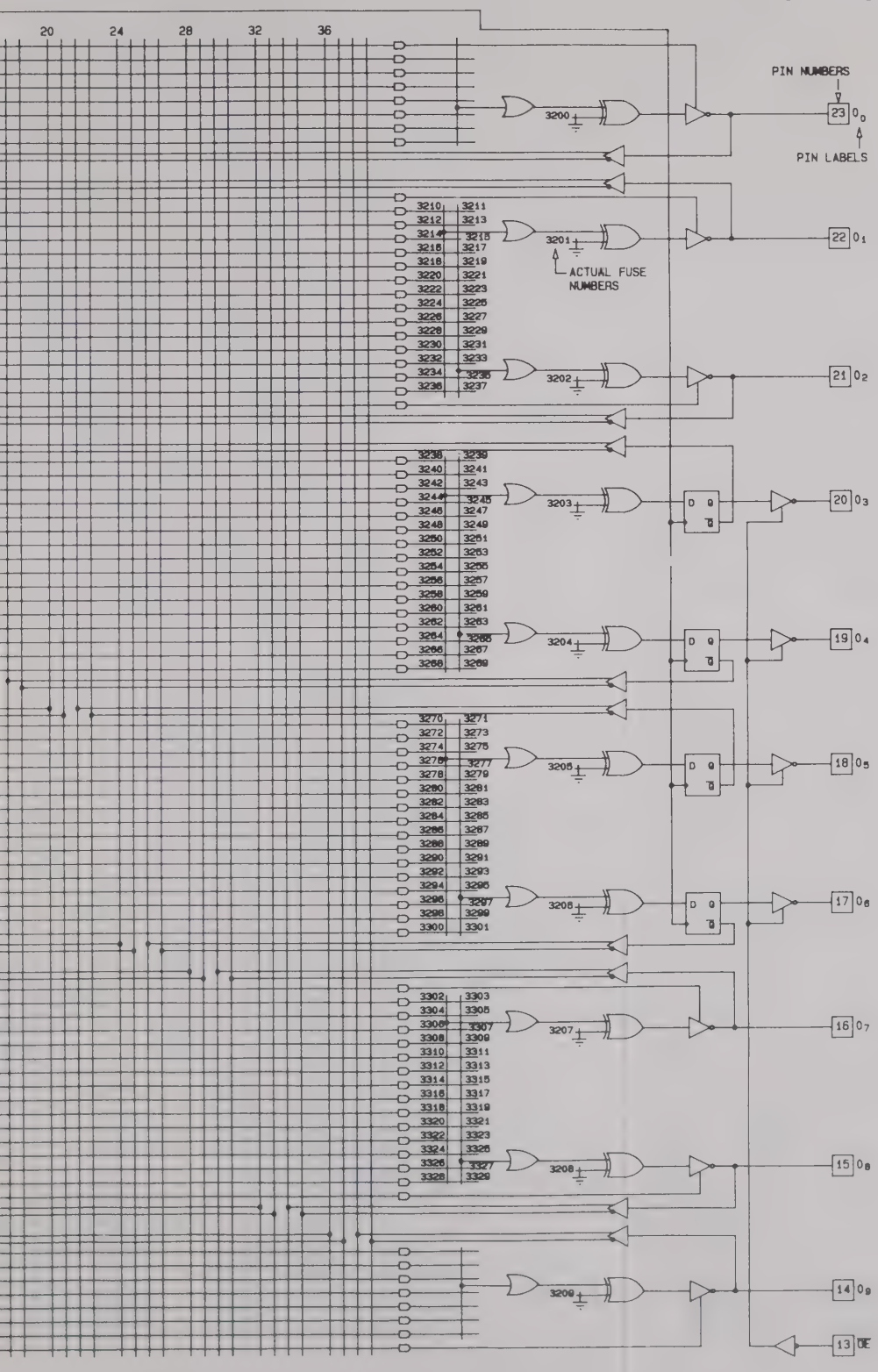
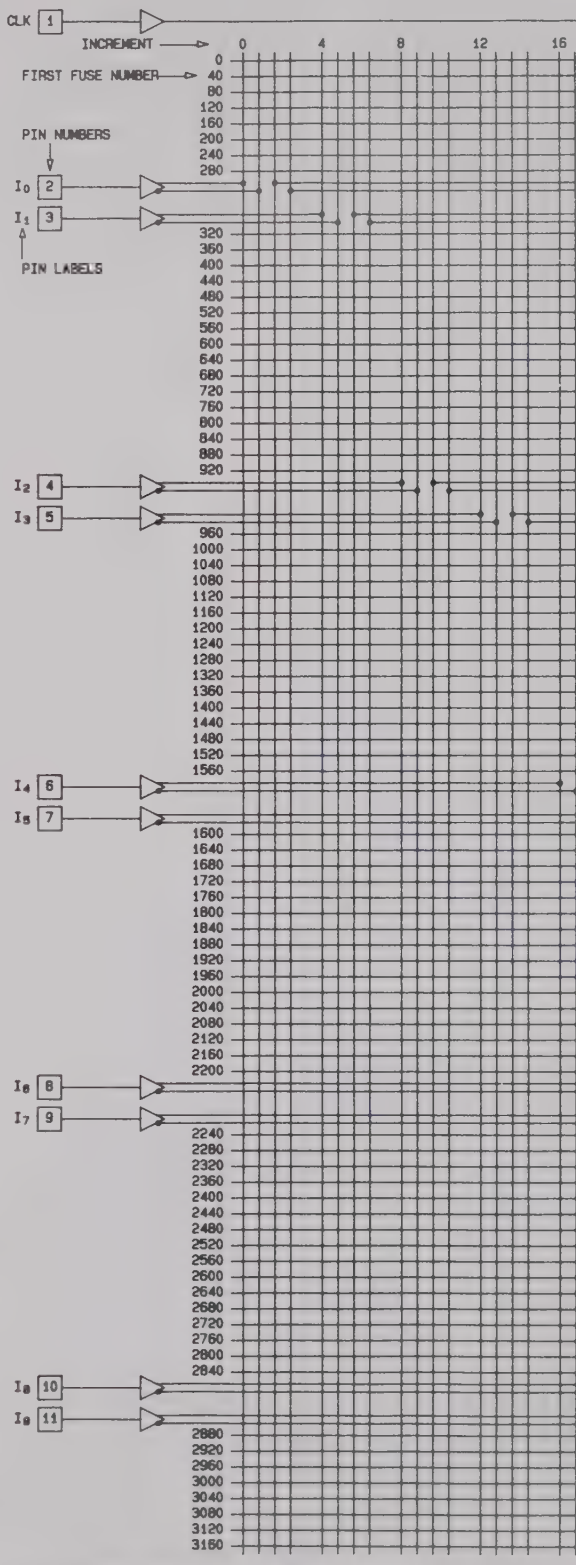
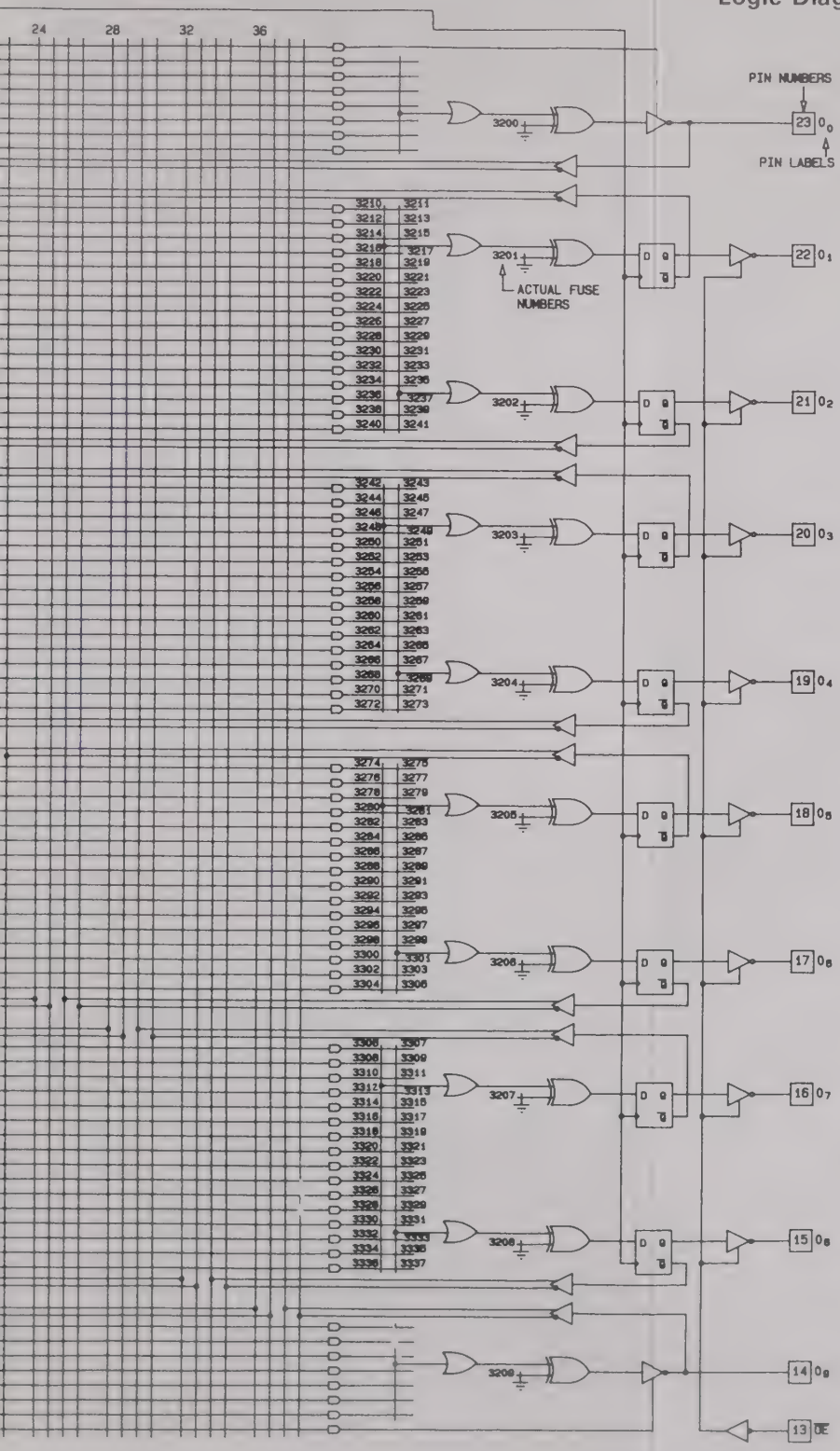


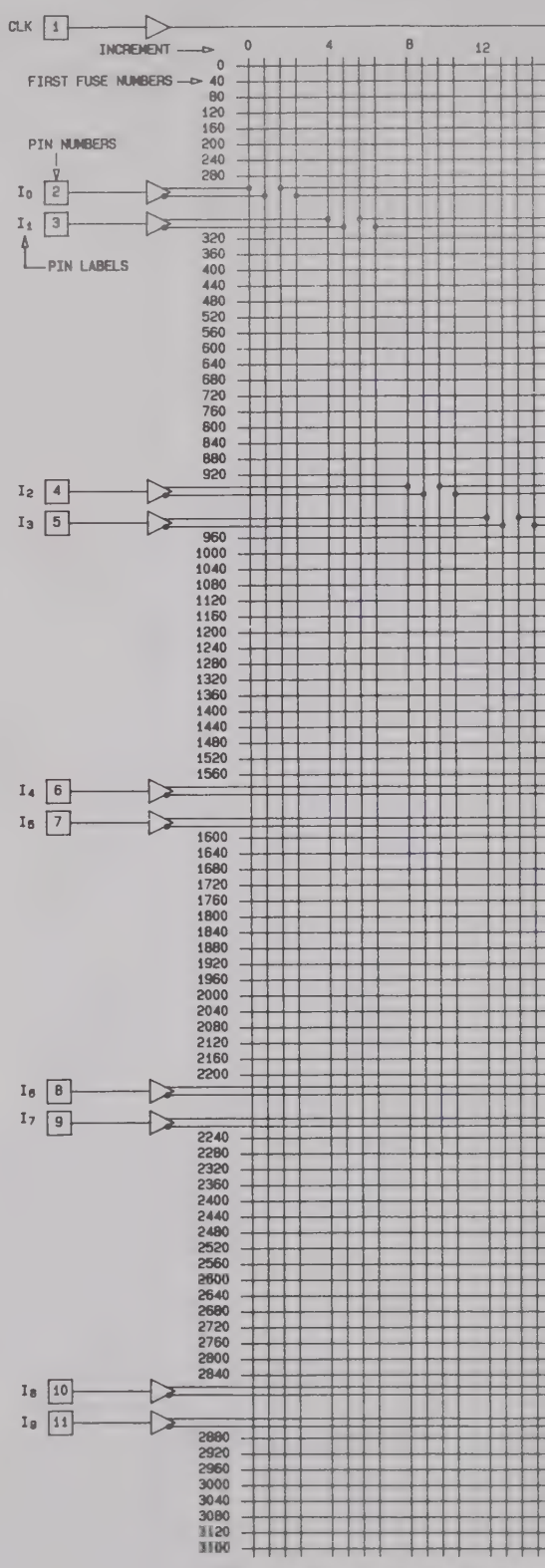
Figure A-34. Logic Diagram PAL20RS4



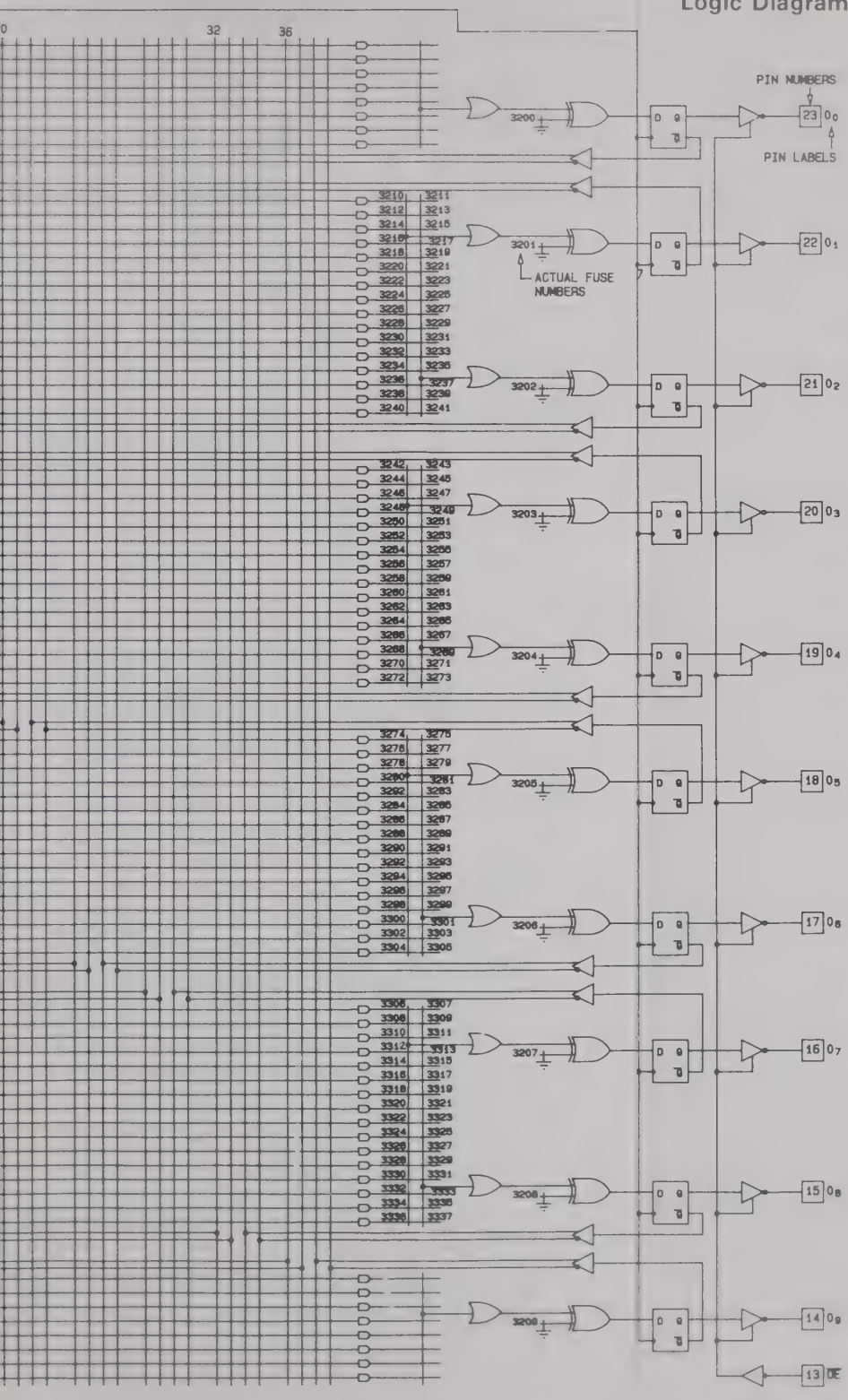
NOTE: FUSE NUMBER =FIRST FUSE NUMBER+ INCREMENT



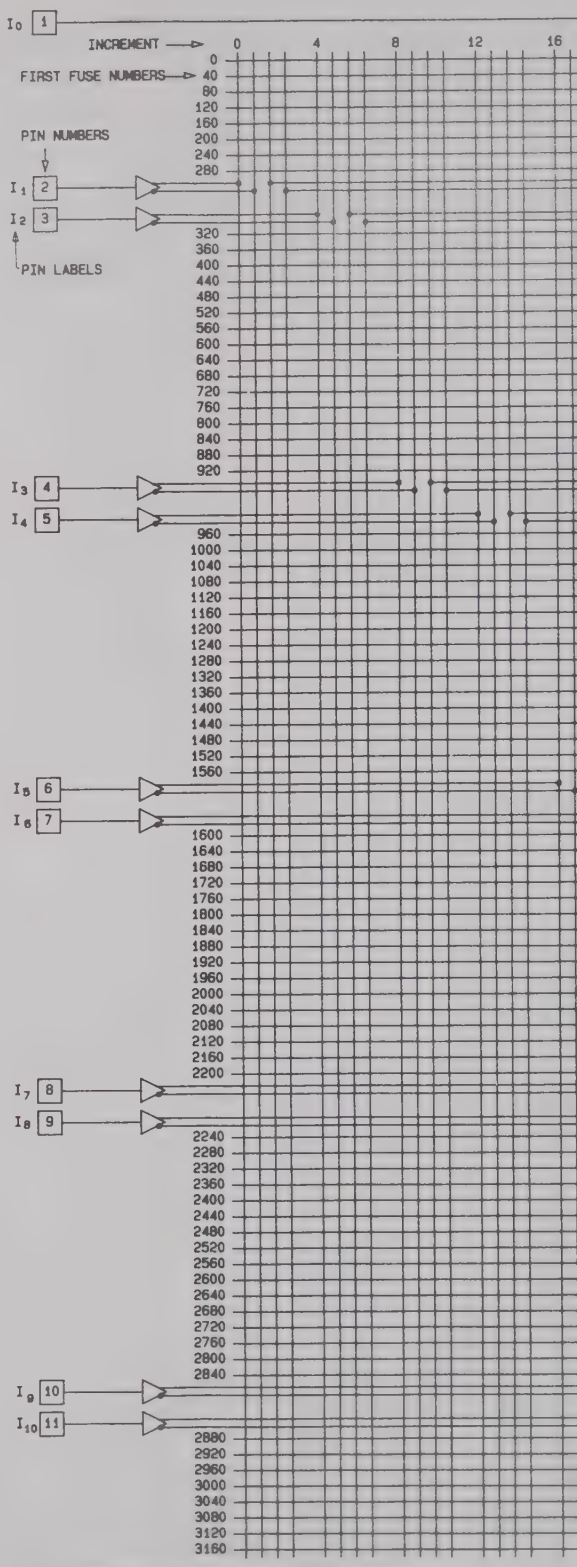
35. Logic Diagram PAL20RS8


CLK 1
INCREMENT
0
4
8
12
FIRST FUSE NUMBERS
0
40
80
120
160
200
240
280
PIN NUMBERS
I0 2
I1 3
PIN LABELS
320
360
400
440
480
520
560
600
640
680
720
760
800
840
880
920
I2 4
I3 5
960
1000
1040
1080
1120
1160
1200
1240
1280
1320
1360
1400
1440
1480
1520
1560
I4 6
I5 7
1600
1640
1680
1720
1760
1800
1840
1880
1920
1960
2000
2040
2080
2120
2160
2200
I6 8
I7 9
2240
2280
2320
2360
2400
2440
2480
2520
2560
2600
2640
2680
2720
2760
2800
2840
I8 10
I9 11
2880
2920
2960
3000
3040
3080
3120
3160
NOTE: FUSE NUMBER = FIRST FUSE NUMBER + I

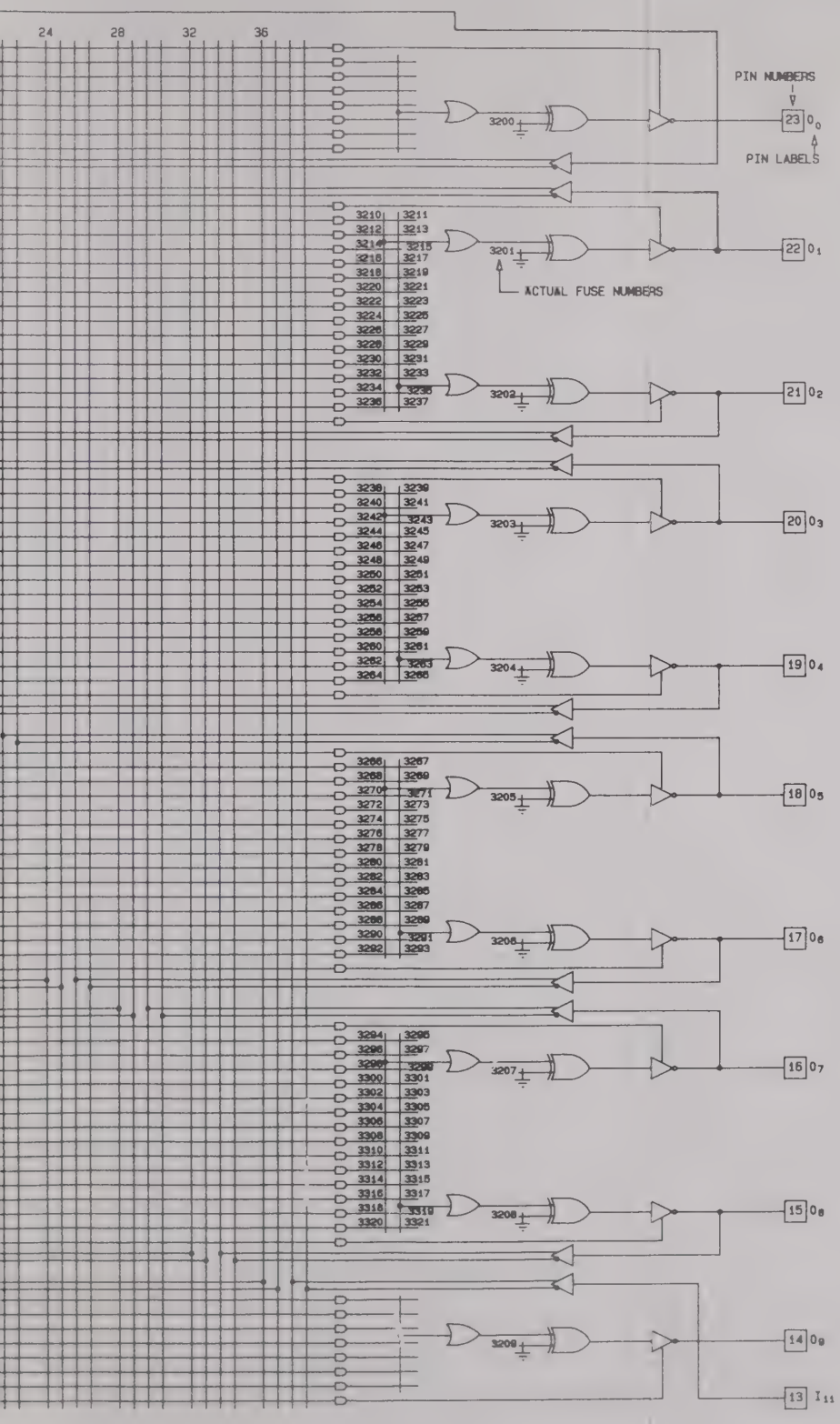
Logic Diagram PAL20RS10



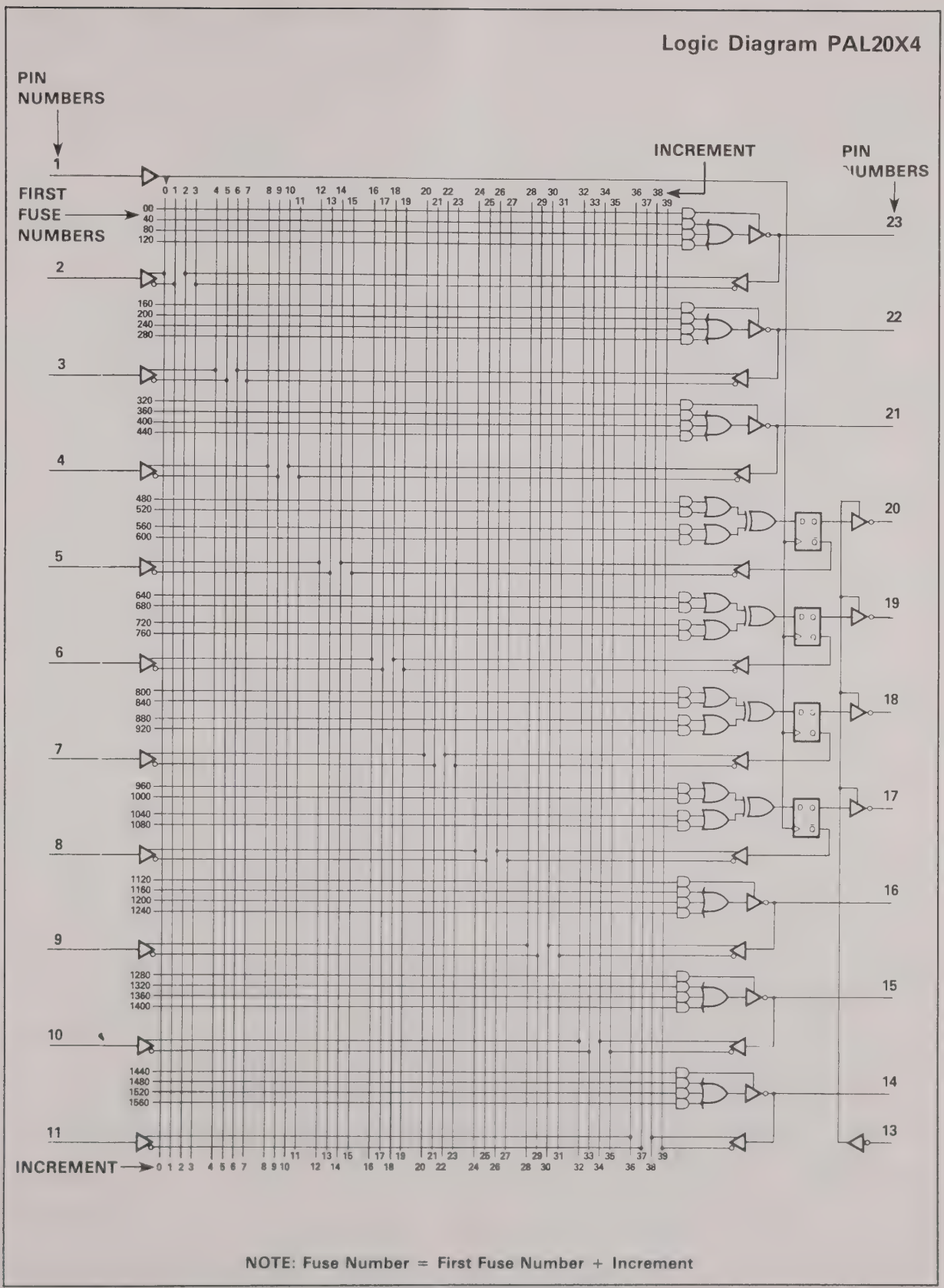
A-36. Logic Diagram PAL20RS10



NOTE: FUSE NUMBER = FIRST FUSE NUMBER + INCREMENT



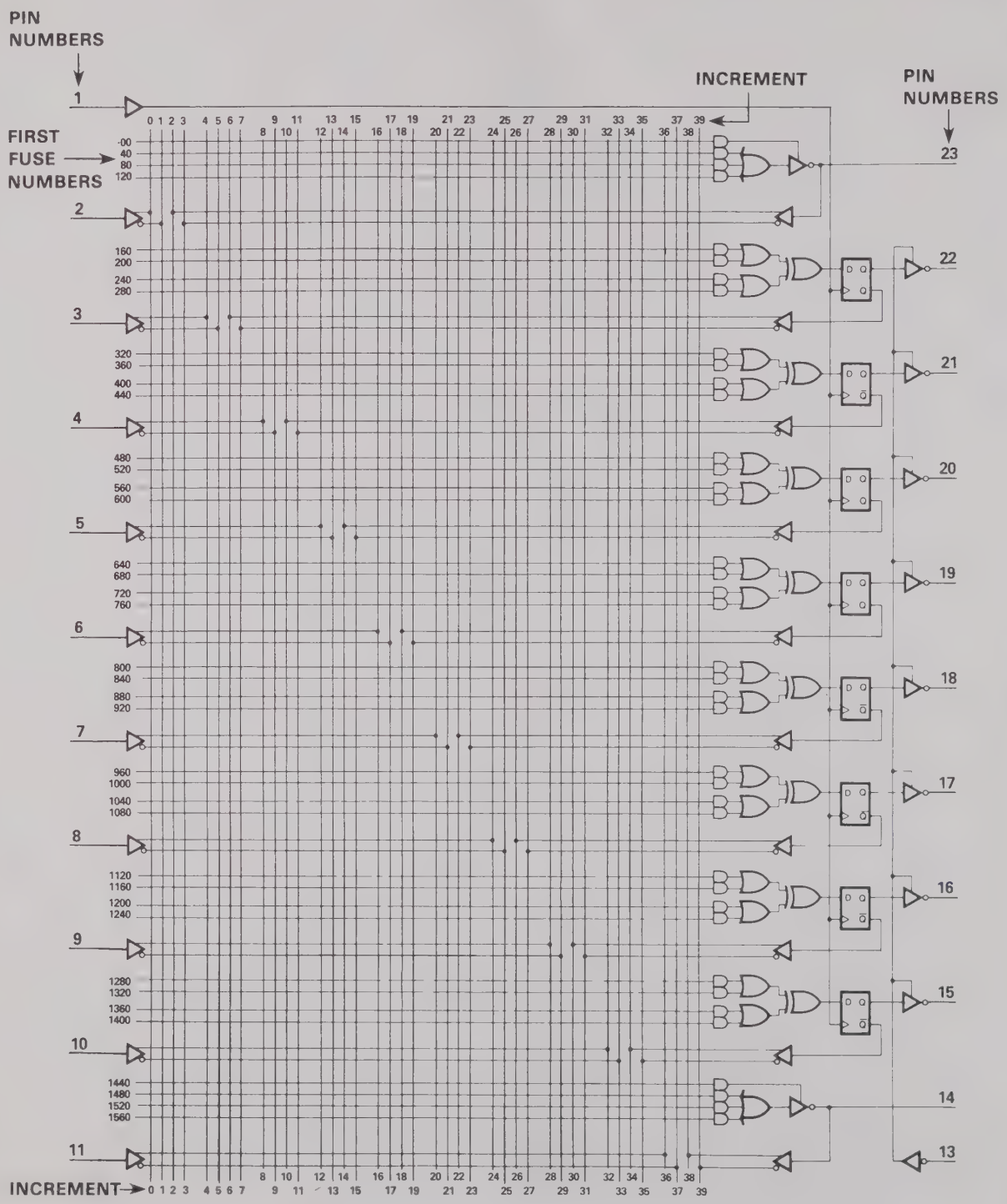
A-37. Logic Diagram PAL20S10



NOTE: Fuse Number = First Fuse Number + Increment

Figure A-38. Logic Diagram PAL20X4

Logic Diagram PAL20X8



NOTE: Fuse Number = First Fuse Number + Increment

Figure A-39. Logic Diagram PAL20X8

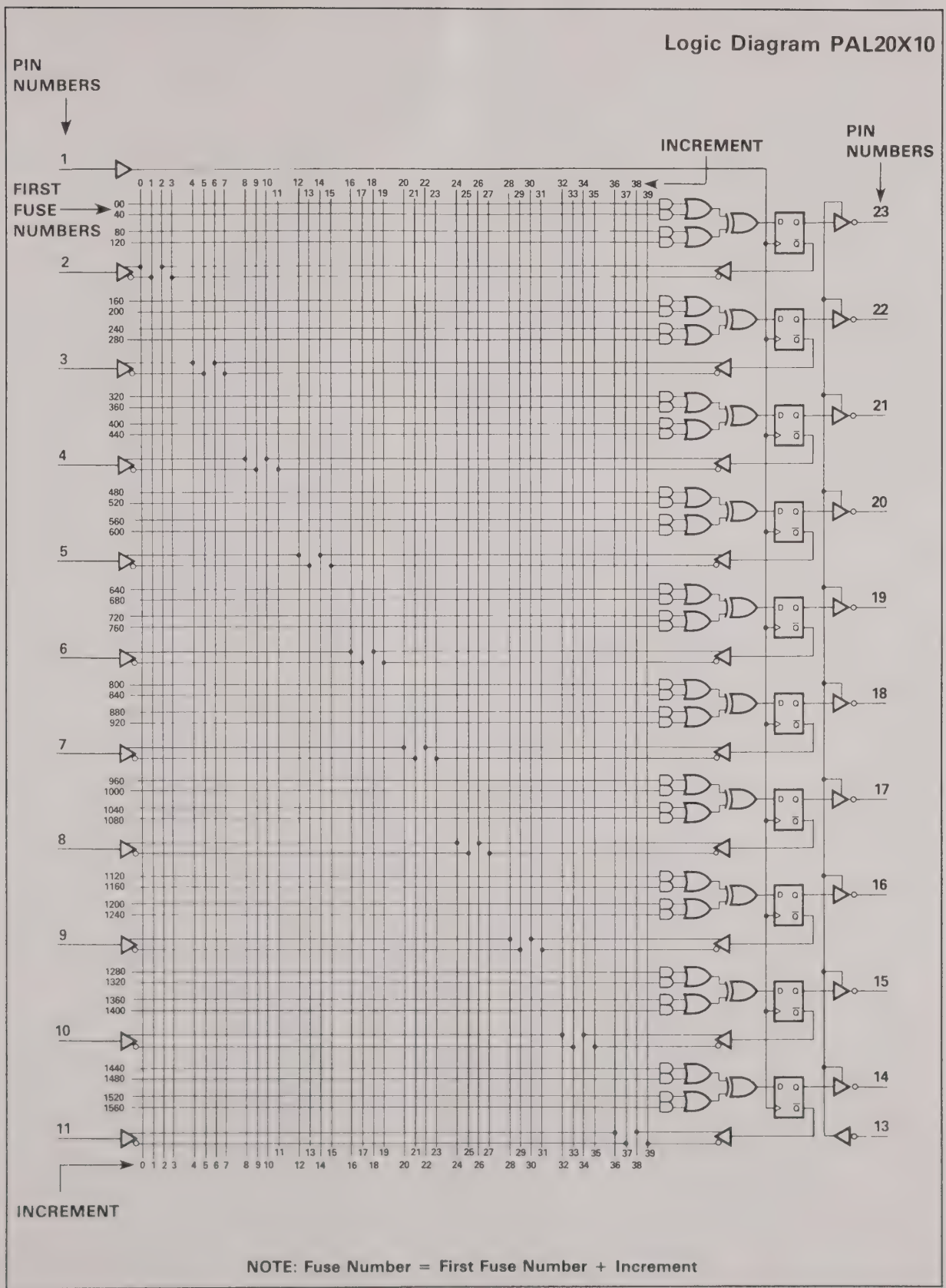
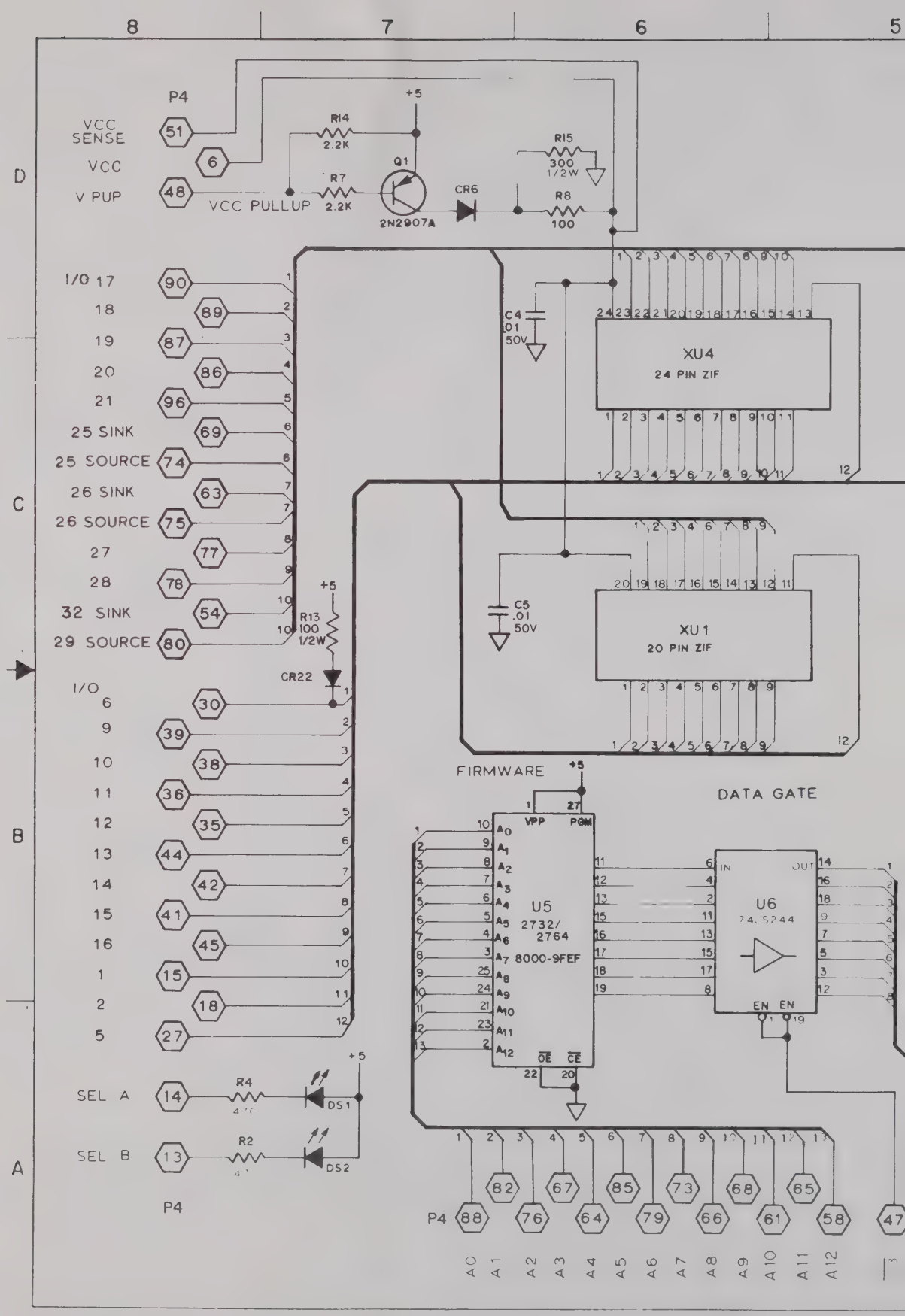


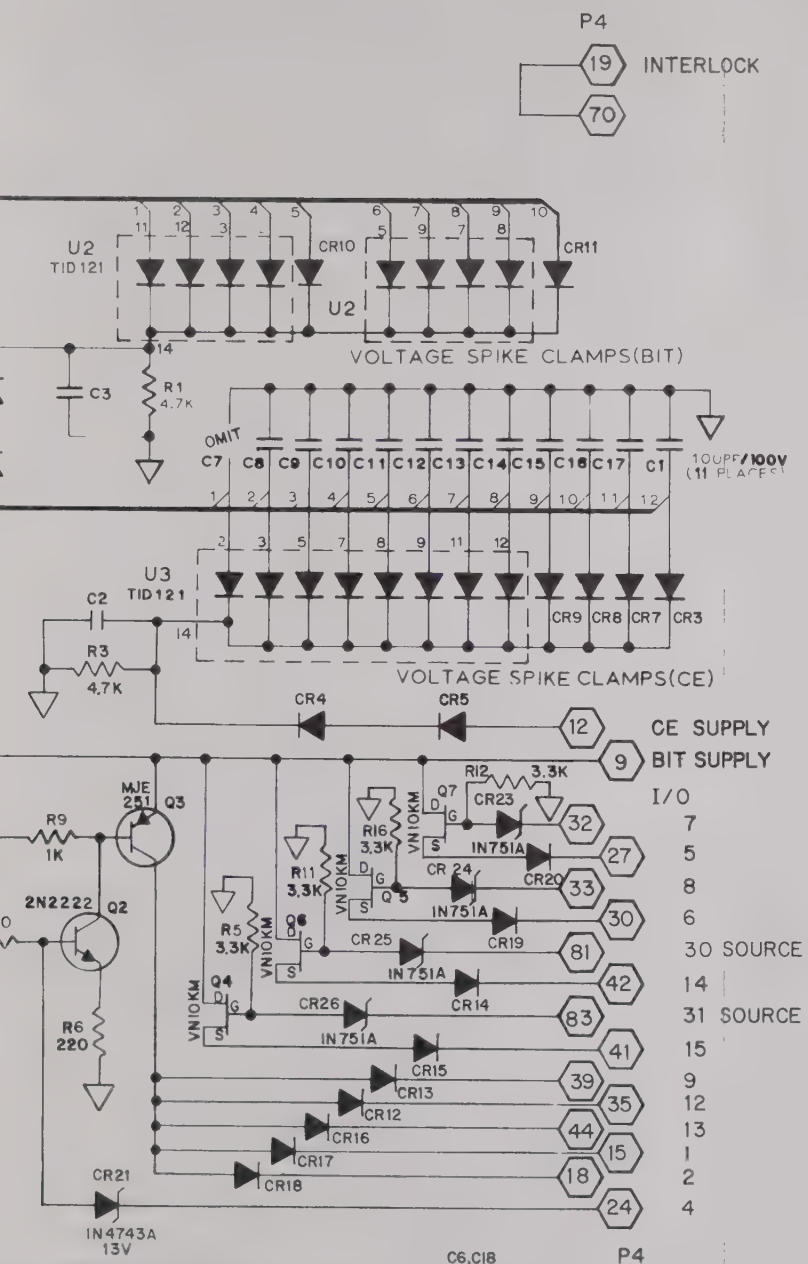
Figure A-40. Logic Diagram PAL20X10

APPENDIX B
SCHEMATIC

30-701-0130 Programming/Testing Adapter


8
7
6
5
D
C
B
A
P4
VCC SENSE
VCC
V PUP
51
6
48
R14
2.2K
R7
2.2K
VCC PULLUP
+5
Q1
2N2907A
CR6
R15
300
1/2W
R8
100
I/O 17
18
19
20
21
25 SINK
25 SOURCE
26 SINK
26 SOURCE
27
28
32 SINK
29 SOURCE
90
89
87
86
96
69
74
63
75
77
78
54
80
C4
.01
50V
XU4
24 PIN ZIF
C5
.01
50V
XU1
20 PIN ZIF
R13
100
1/2W
CR22
I/O
6
9
10
11
12
13
14
15
16
1
2
5
30
39
38
36
35
44
42
41
45
15
18
27
SEL A
SEL B
14
13
R4
R2
DS1
DS2
FIRMWARE
DATA GATE
U5
2732/
2764
8000-9FEF
VPP
PGM
OE
CE
U6
74LS244
IN
OUT
EN
P4
88
76
64
79
66
61
58
47
82
67
85
73
68
65
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
A12

REVISIONS					
LTR	DESCRIPTION	DR	CHK	APPR'D	DATE
A	RELEASE	LH	[illegible]	HA	5-4-84
B	INCORP. ADCN B1 PER ECP 0044	LH	[illegible]	[illegible]	9-29-84



NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL RESISTORS ARE 1/4W AND IN OHMS, 5%.
2. ALL CAPACITORS ARE IN MICROFARADS, .1, 50V.
3. LAST REFERENCE DESIGNATOR USED: C19, CR22, DS2, P4, R16, U6, Q7.
4. ALL DIODES 1N4148.
5. POWER & GROUND.

REF DES	+5	GND
XU4	-	12
XU1	-	10
U6	20	10
U5	26,28	14

P/N 701-0130-002

APPROVALS		UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	DATA I/O	
DSN ENGR K. Mell	DATE 5/4/84	TOLERANCES UNLESS OTHERWISE SPECIFIED XX ±.xx ANGULAR	TITLE SCHEMATIC DIAGRAM, TEST PROG ADAPTER	
MFG ENGR	DATE			
QUAL ASSUR E. Braithwaite	DATE 5/4/84	DRAWN BY L. Humble	DATE 12-7-83	SIZE D
ENGR MGR	DATE 5/4/84	CHECKED BY [illegible]	DATE 5/4/84	DRAWING NO 30-701-0130
				SHEET 1 OF 1

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